SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer and Demultiplexer 2.5V and 3.3V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-bandwidth data path (up to 500MHz)
- 5V Tolerant I/Os with device powered up or powered down
- Low and flat on-state resistance (r_{on}) characteristics over operating range (r_{on}= 4Ω typical)
- Rail-to-rail switching on data I/O ports
  - 0- to 5V Switching with 3.3V V_{CC}
  - 0- to 3.3V Switching with 2.5V V_{CC}
- Bidirectional data flow with near-zero propagation delay
- Low input and output capacitance minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5pF typical)
- Fast switching frequency (f $\overline{OE}$ = 20MHz maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 0.7mA typical)
- V_{CC} Operating range from 2.3V to 3.6V
- Data I/Os support 0- to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V and 3.3V CMOS outputs
- I_{off} Supports partial-power-down mode operation
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD Performance tested per JESD 22
  - 2000V Human body model (A114B, class II)
  - 1000V Charged-device model (C101)
- Supports both digital and analog applications: USB interface, differential signal interface, bus isolation, low-distortion signal gating [1]

2 Applications

- IP Phones: wired and wireless
- Optical modules
- Optical networking: video over fiber and EPON
- Private branch exchange (PBX)
- WiMAX and wireless infrastructure equipment

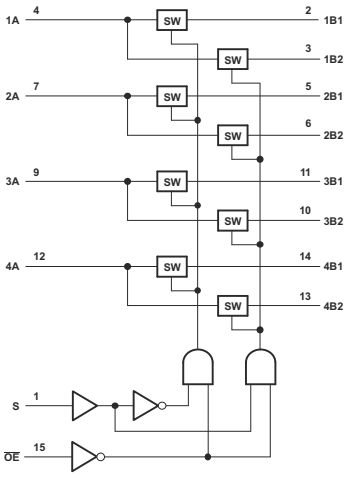
3 Description

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74CB3Q3257	TVSOP (DGV, 16)	3.6mm × 6.4mm
	SSOP (DBQ, 16)	4.9mm × 6mm
	TSSOP (PW, 16)	5mm × 6.4mm
	VQFN (RGV, 16)	4mm × 3.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

[1] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI *CBT-C, CB3T, and CB3Q Signal-Switch Families* application report.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

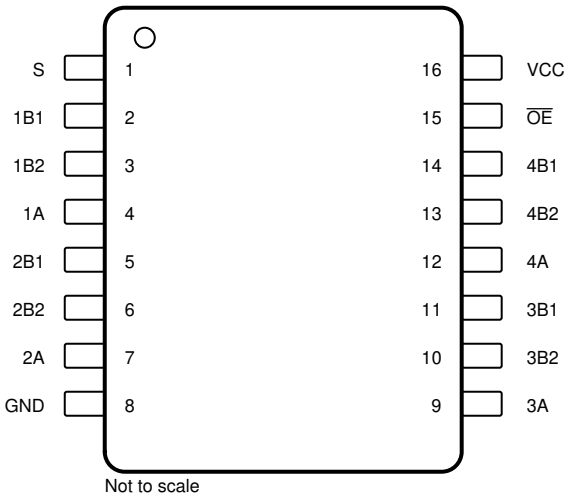


Figure 4-1. DYY, DGV, DBQ, or PW Package 16-Pin SOT-23 THN, TVSOP, SSOP, or TSSOP (Top View)

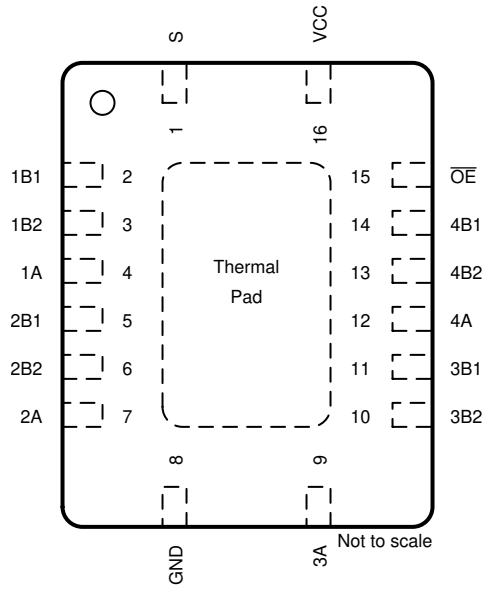


Figure 4-2. RGY Package, 16-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
S	1	I	Select Pin
1B1	2	I/O	Channel 1I/O 1
1B2	3	I/O	Channel 1I/O 2
1A	4	I/O	Channel 1 common
2B1	5	I/O	Channel 2I/O 1
2B2	6	I/O	Channel 2I/O 2
2A	7	I/O	Channel 2 common
GND	8	—	Ground
3A	9	I/O	Channel 3 common
3B2	10	I/O	Channel 3I/O 2
3B1	11	I/O	Channel 3I/O 1
4A	12	I/O	Channel 4 common
4B2	13	I/O	Channel 4I/O 2
4B1	14	I/O	Channel 4I/O 1
$\overline{OE}$	15	I	Output Enable (Active Low)
V_{CC}	16	—	Power

(1) I = Input; I/O = Input or Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
I_{IO}	ON-state switch current			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature	PKG = RGY, DBQ, DGV, PW	–40	105	°C
T_A	Operating free-air temperature	PKG = DYY	-40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to provide proper device operation. See also the *Implications of Slow or Floating CMOS Inputs* application note.

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5.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3257					UNIT
		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DYY (SOT-23-THN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.4	134.2	114.3	72.3	126.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.1	66.1	57.9	71.9	14.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	62.7	80.1	72.2	47.1	72.8	
ψ_{JT}	Junction-to-top characterization parameter	18.7	17.7	16.3	19.5	73.0	
ψ_{JB}	Junction-to-board characterization parameter	64.6	79.6	71.8	47.2	71.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	31.4	-	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics - PKG = RGY, PW, DBQ, DGV

T_A = –40°C to 105°C. Typical values stated are over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6V, I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V, V_{IN} = 0 to 5.5V				±1	µA
I_{OZ} (3)		V_{CC} = 3.6V, V_O = 0 to 5.5V, V_I = 0, Switch OFF V_{IN} = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5V, V_I = 0				1	µA
I_{CC}		V_{CC} = 3.6V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND			0.7	1.5	mA
ΔI_{CC} (4)	Control inputs	V_{CC} = 3.6V, One input at 3V, Other inputs at V_{CC} or GND				30	µA
I_{CCD} (5)	Per control input	V_{CC} = 3.6V, A and B ports open, Control input switching at 50% duty cycle			0.4	0.5	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3V, V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			5.5	7	pF
	B port	V_{CC} = 3.3V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			3.5	5	pF
$C_{io(ON)}$	A port	V_{CC} = 3.3V, Switch ON, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			10.5	13	pF
	B port				10.5	13	
r_{on} (6)		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0, I_O = 30mA		4	8	Ω
			V_I = 1.7V, I_O = –15mA		4	9	
		V_{CC} = 3V	V_I = 0, I_O = 30mA		4	6	
			V_I = 2.4V, I_O = –15mA		4	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data terminals.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 5-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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5.6 Electrical Characteristics - PKG = DYY

T_A = –40°C to 105°C. Typical values stated are over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6V, I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V, V_{IN} = 0 to 5.5V				±1	µA
I_{OZ} (3)		V_{CC} = 3.6V, V_O = 0 to 5.5V, V_I = 0, Switch OFF V_{IN} = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5V, V_I = 0				1	µA
I_{CC}		V_{CC} = 3.6V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND			0.5	1.5	mA
ΔI_{CC} (4)	Control inputs	V_{CC} = 3.6V, One input at 3V, Other inputs at V_{CC} or GND				30	µA
I_{CCD} (5)	Per control input	V_{CC} = 3.6V, A and B ports open, Control input switching at 50% duty cycle			0.32	0.5	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3V, V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			5.5	7	pF
	B port	V_{CC} = 3.3V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			3.5	5	pF
$C_{io(ON)}$	A port	V_{CC} = 3.3V, Switch ON, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5V, 3.3V, or 0			10.5	13	pF
	B port				10.5	13	
r_{on} (6)		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0, I_O = 30mA		4	8	Ω
			V_I = 1.7V, I_O = –15mA		5.3	9	
		V_{CC} = 3V	V_I = 0, I_O = 30mA		3.5	6	
			V_I = 2.4V, I_O = –15mA		4	8	

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5.7 Switching Characteristics, V_{CC} = 2.5V, PKG = RGY, DGV, DBQ, PW

Typical values stated are over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V			UNIT
			MIN	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10	10	MHz
t_{pd} (2)	A or B	B or A		0.12	0.21	ns
$t_{pd(s)}$	S	A	1.5	6.5	7.5	ns
t_{en}	S	B	1.5	6.5	7.5	ns
	$\overline{OE}$	A or B	1.5	6.5	7.5	
t_{dis}	S	B	1	6	7	ns
	$\overline{OE}$	A or B	1	6	7	

(1) Maximum switching frequency for control inputs ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

5.8 Switching Characteristics, V_{CC} = 2.5V, PKG = DYY

Typical values stated are over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V			UNIT
			MIN	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10	10	MHz
t_{pd} (2)	A or B	B or A		0.12	0.21	ns
$t_{pd(s)}$	S	A	1.5	6.5	8.5	ns
t_{en}	S	B	1.5	6.5	8.5	ns
	$\overline{OE}$	A or B	1.5	6.5	8.5	
t_{dis}	S	B	1	6	8	ns
	$\overline{OE}$	A or B	1	6	8	

5.9 Switching Characteristics, V_{CC} = 3.3V, PKG= RGY, PW, DGV, DBQ

Typical values stated are over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3V ± 0.3V				UNIT
			MIN	TYP(1)	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B			20	20	MHz
t_{pd} (2)	A or B	B or A			0.2	0.32	ns
$t_{pd(s)}$	S	A	1.5	4.1	5.5	6.5	ns
t_{en}	S	B	1.5	4.6	5.5	6.5	ns
	$\overline{OE}$	A or B	1.5	4.7	5.5	6.5	
t_{dis}	S	B	1	3.3	6	7	ns
	$\overline{OE}$	A or B	1	3.1	6	7	

(1) TYP taken from average in 105°C

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5.10 Switching Characteristics, V_{CC} = 3.3V, PKG= DYY

Typical values stated are over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3V ± 0.3V				UNIT
			MIN	TYP(1)	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B			20	20	MHz
t_{pd} (2)	A or B	B or A			0.2	0.32	ns
$t_{pd(s)}$	S	A	1.5	4.1	5.5	7.5	ns
t_{en}	S	B	1.5	4.6	5.5	7.5	ns
	$\overline{OE}$	A or B	1.5	4.7	5.5	7.5	
t_{dis}	S	B	1	3.3	6	8	ns
	$\overline{OE}$	A or B	1	3.1	6	8	

5.11 Typical Characteristics

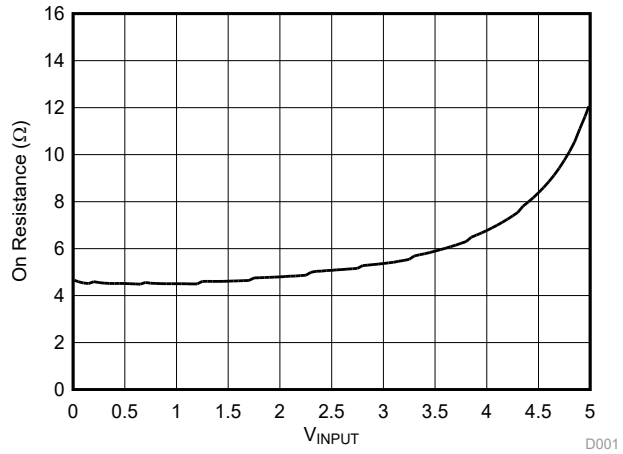


Figure 5-1. Typical R_{on} (On Resistance) vs V_{INPUT} , V_{CC} = 3.3V, T_A = 25°C, I_O = 15mA

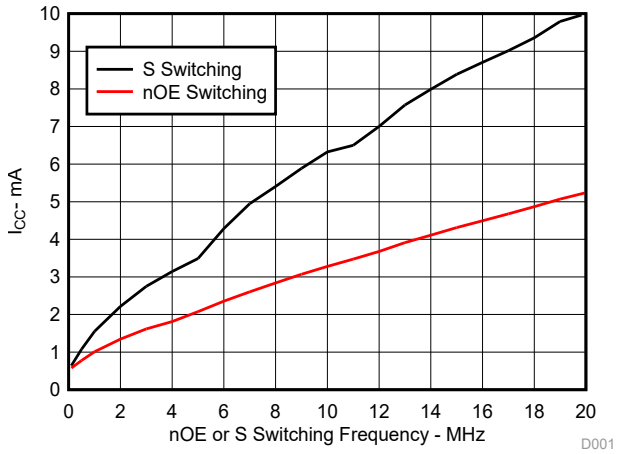
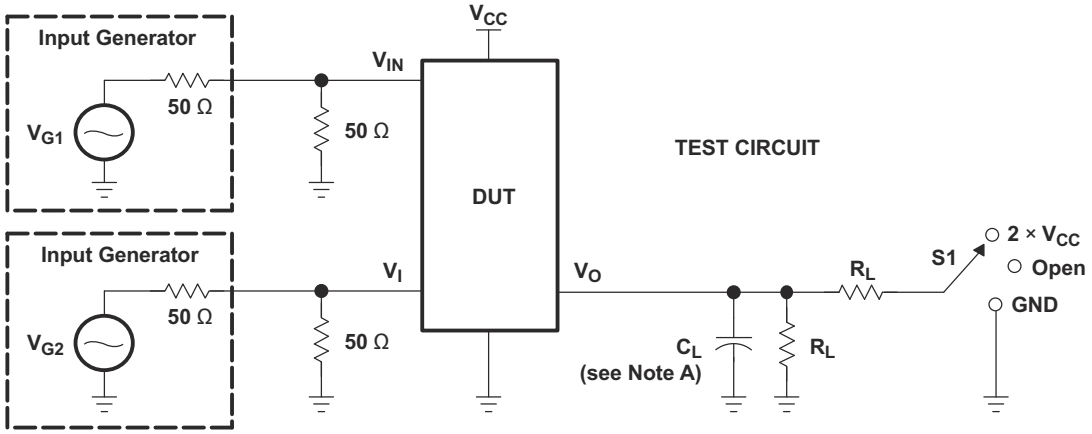


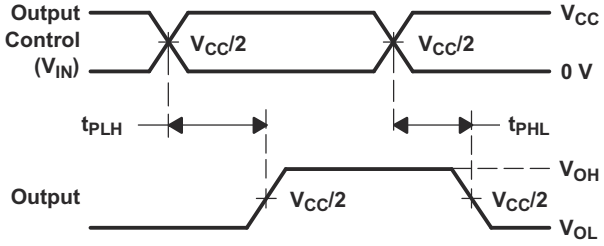
Figure 5-2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency , V_{CC} = 3.3V, T_A = 25C, A and B Ports Open

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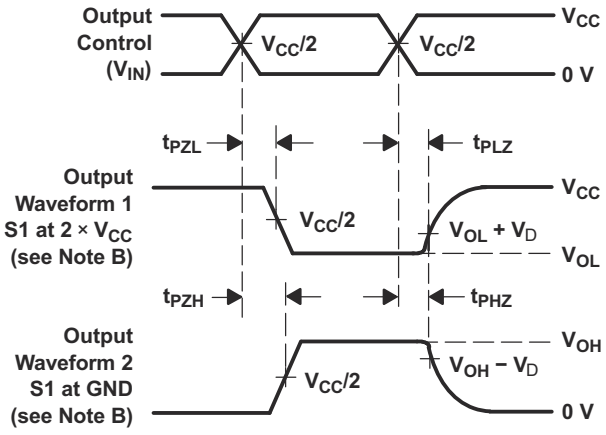
6 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

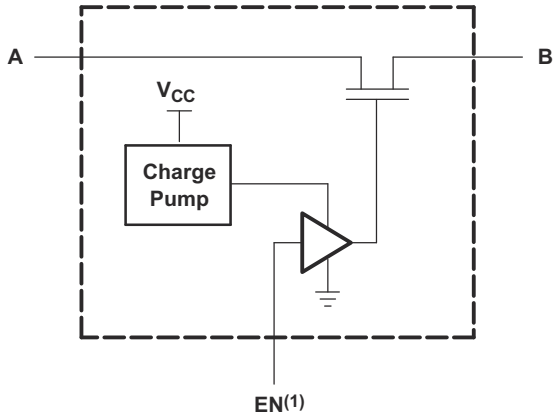
7.1 Overview

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 device provides an optimized interface device designed for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable (1 $\overline{OE}$, 2 $\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when the device is powered down. The device has isolation during power off.

To provide the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

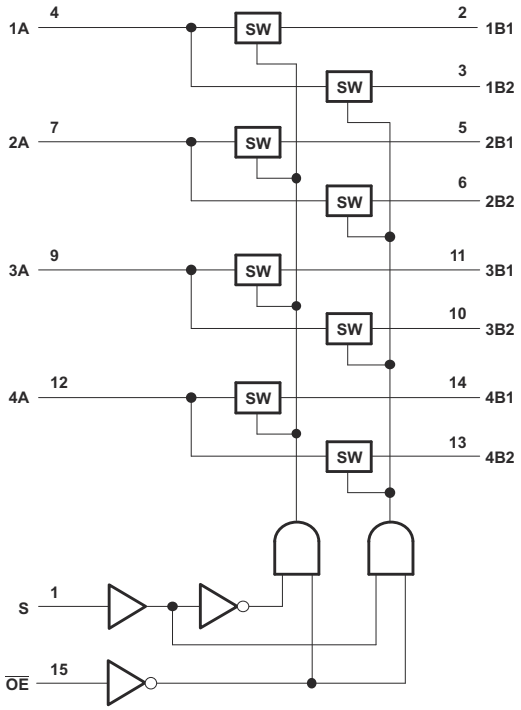


(1) EN is the internal enable signal applied to the switch.

Figure 7-1. Simplified Schematic, Each FET Switch (SW)

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7.2 Functional Block Diagram



7.3 Feature Description

The SN74CB3Q3257 device has a high-bandwidth data path (up to 500MHz) and has 5V tolerant I/Os with the device powered up or powered down. The device also has low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4Ω Typical).

This device also has rail-to-rail switching on data I/O ports for 0- to 5V switching with 3.3V V_{CC} and 0- to 3.3V switching with 2.5V V_{CC} as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5pF Typical).

The SN74CB3Q3257 also provides a fast switching frequency ($f_{\overline{OE}}$ = 20MHz Max) with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC} = 0.6mA Typical).

The V_{CC} operating range is from 2.3V to 3.6V and the data I/Os support 0 to 5V signal levels of (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V).

The control inputs can be driven by TTL or 5V / 3.3V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74CB3Q3257.

Table 7-1. Function Table

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74CB3Q3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices. the $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a very generic example, and can apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

8.2 Typical Application

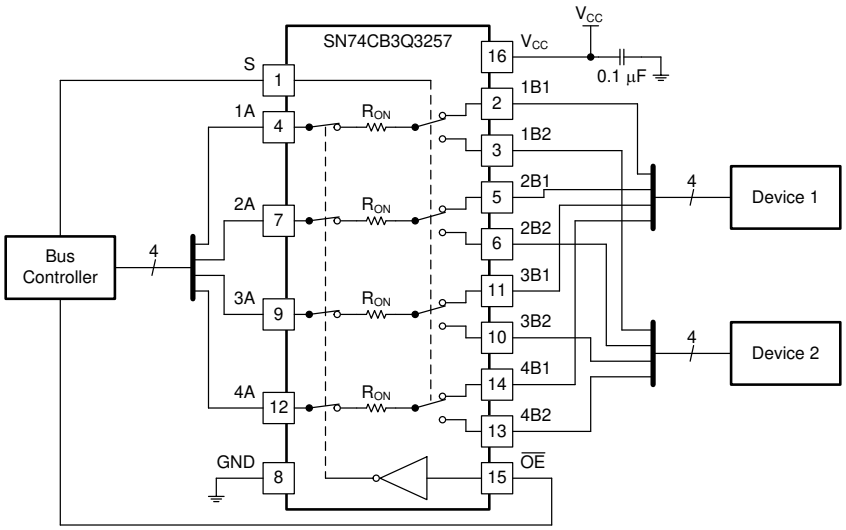


Figure 8-1. Typical Application of the SN74CB3Q3257

8.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 5.3*.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed ±128mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 500MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in *Section 8.4*.

8.2.2 Detailed Design Procedure

The 0.1µF capacitor must be place as close as possible to the device.

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8.2.3 Application Curve

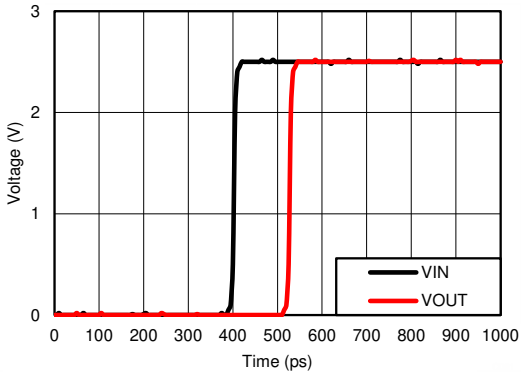


Figure 8-2. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5V.

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Section 5.1* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

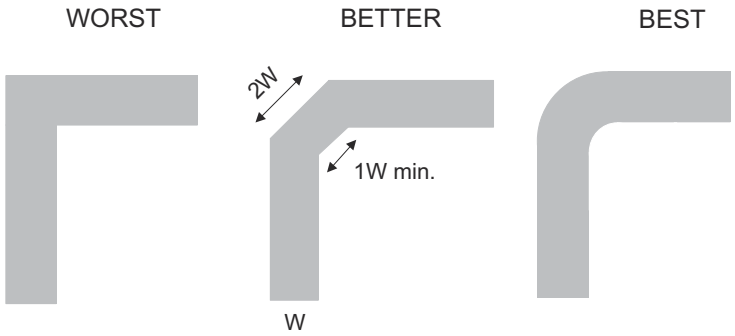


Figure 8-3. Trace Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2024) to Revision F (August 2026) **Page**

- Updated the number formatting for tables, figures, and cross-references throughout the document 1
- Updated the *Thermal Information* table values 5
- Updated the maximum value of the *Per input control* parameter in the *Electrical Characteristics - PKG = RGY, PW, DBQ, DGV* table from 0.35 to 0.45..... 5
- Updated new package information to the *Switching Characteristics* tables 7
- Updated the *Typical Characteristics* section..... 8

Changes from Revision D (July 2018) to Revision E (December 2024) **Page**

- Changed the Device Information table to the *Package Information* table..... 1
- Changed the T_A MAX value from 85°C to 105°C in the *Recommended Operating Conditions* 4

Changes from Revision C (April 2017) to Revision D (July 2018) **Page**

- Changed the pinout images appearance 3
- Added *Thermal Information* table values 5

Changes from Revision B (June 2015) to Revision C (April 2017) **Page**

- Added MAX values for T_A = –40°C to 105°C to the *Electrical Characteristics* table..... 5
- Added MAX values for T_A = –40°C to 105°C to the *Switching Characteristics, V_{CC} = 2.5V* table. 5
- Added separate *Switching Characteristics, V_{CC} = 3.3V* for V_{CC} = 3.3V ± 0.3V. Added TYP values and MAX values for T_A = –40°C to 105°C..... 7

Changes from Revision A (November 2003) to Revision B (June 2015) **Page**

- Removed *Ordering Information* table..... 1
- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3Q3257DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

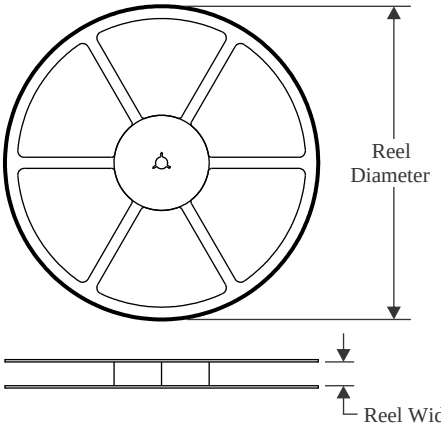
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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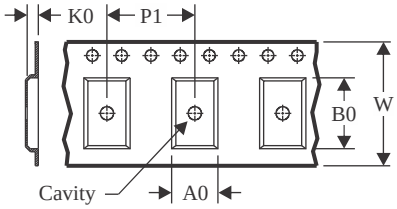
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

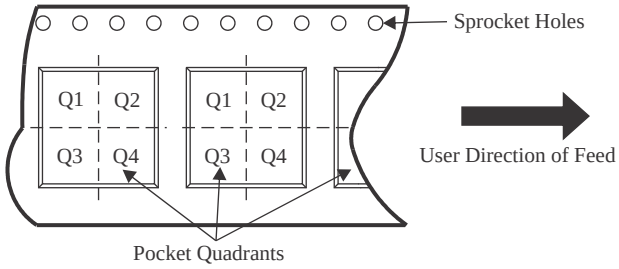


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

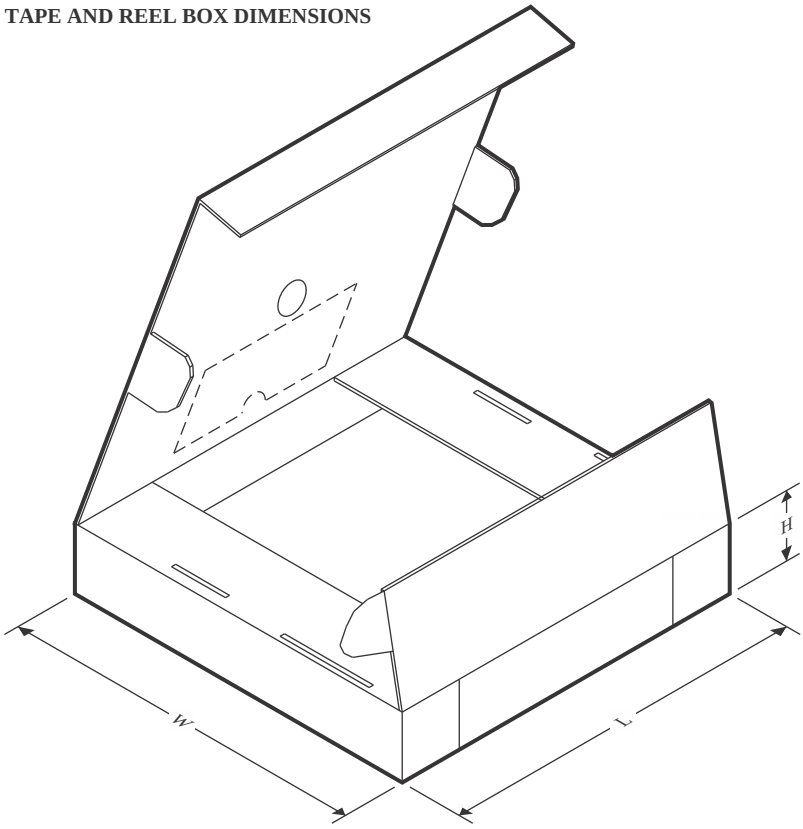
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

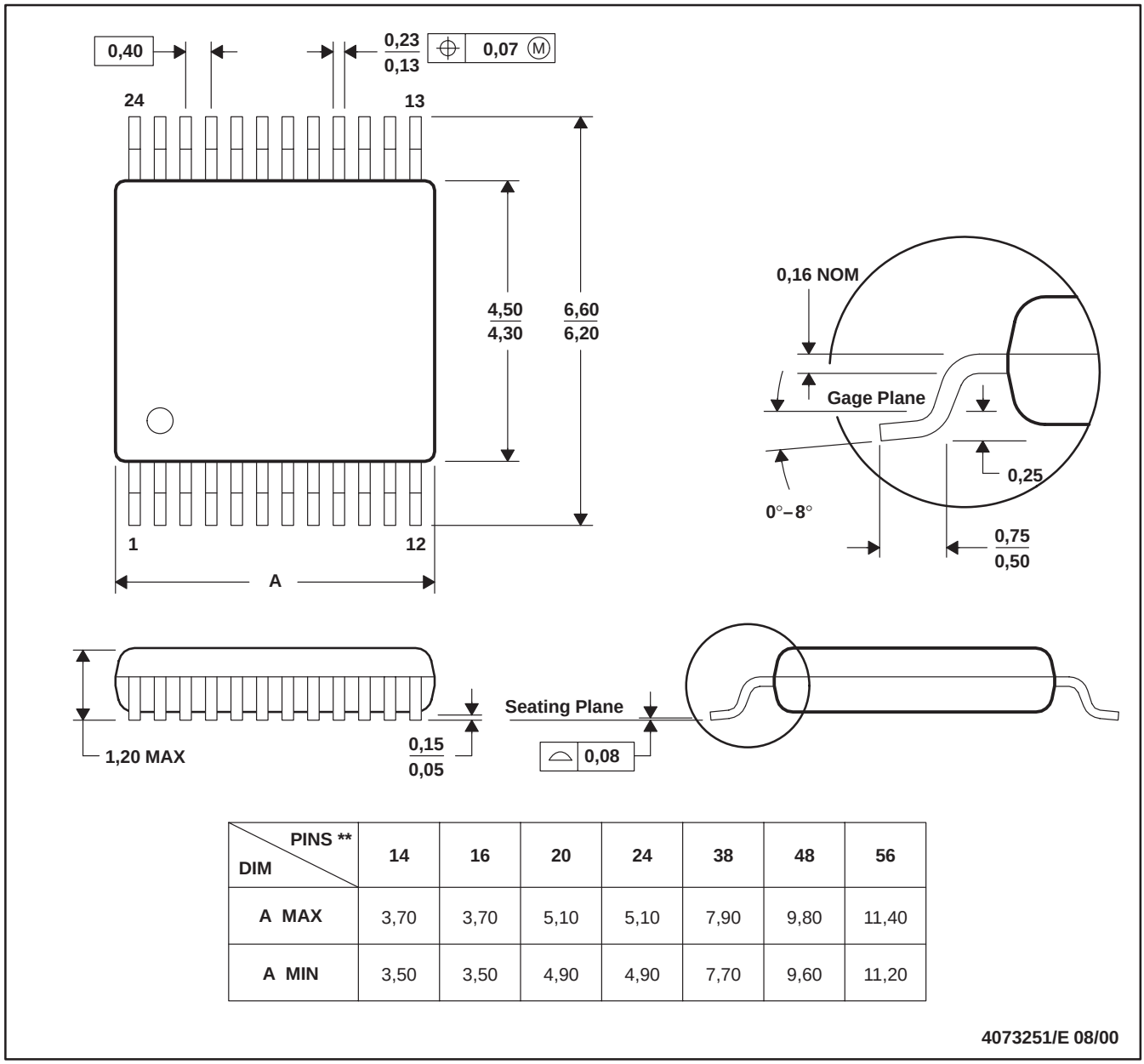


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	360.0	360.0	36.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

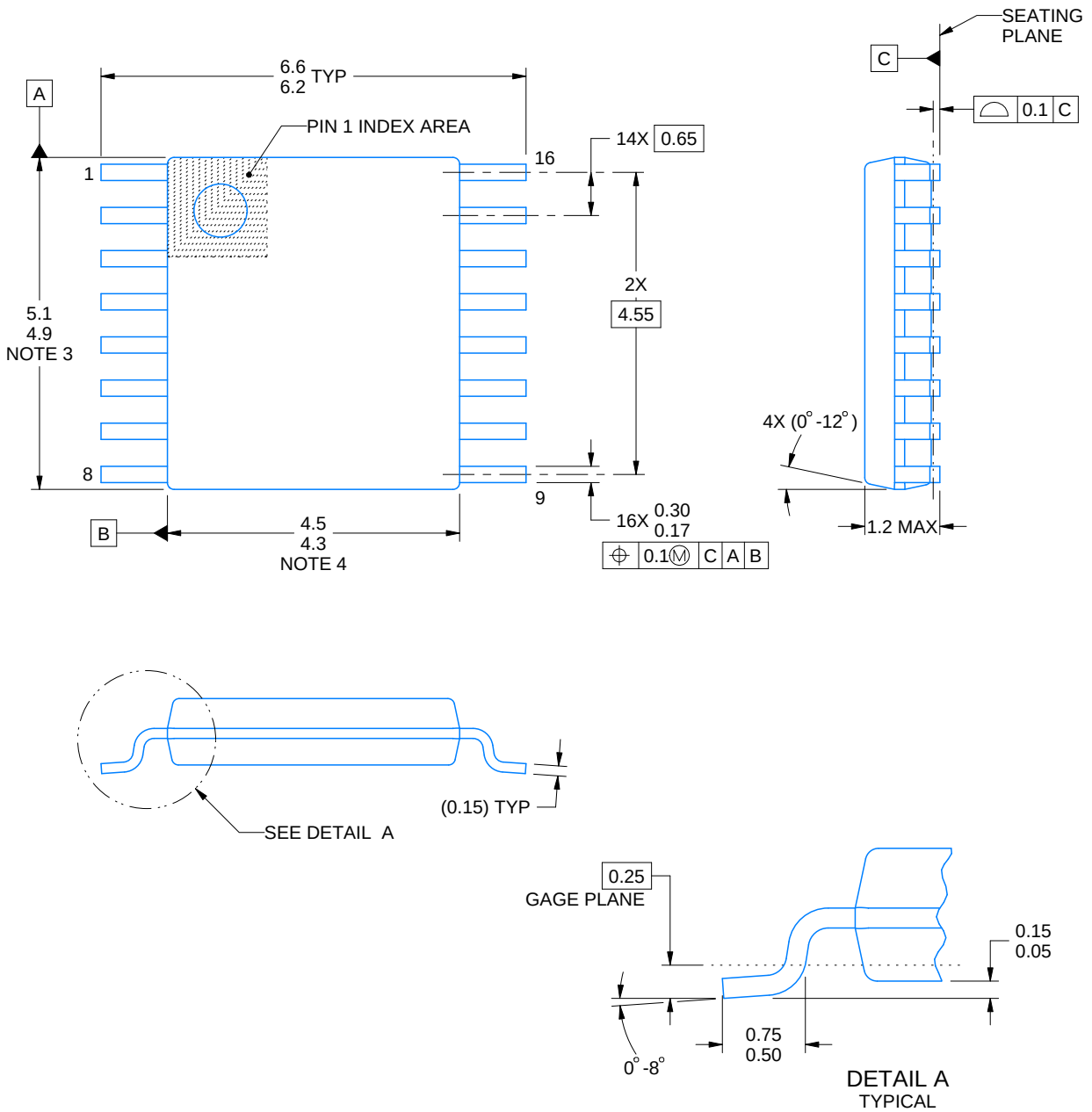
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

PW0016A

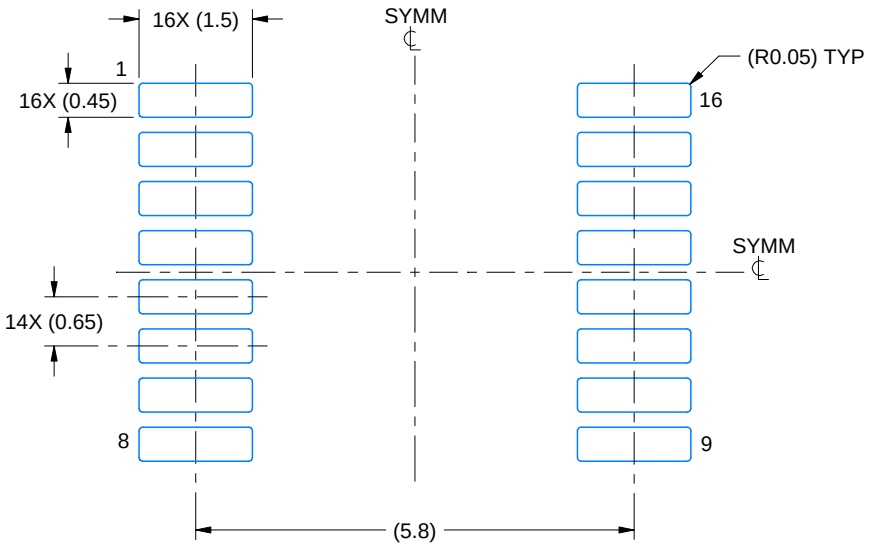
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

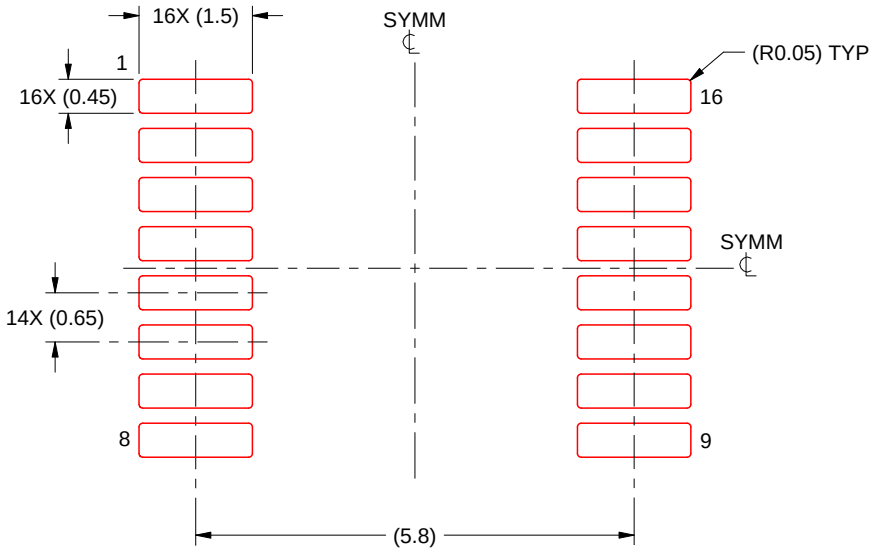


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

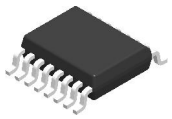


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

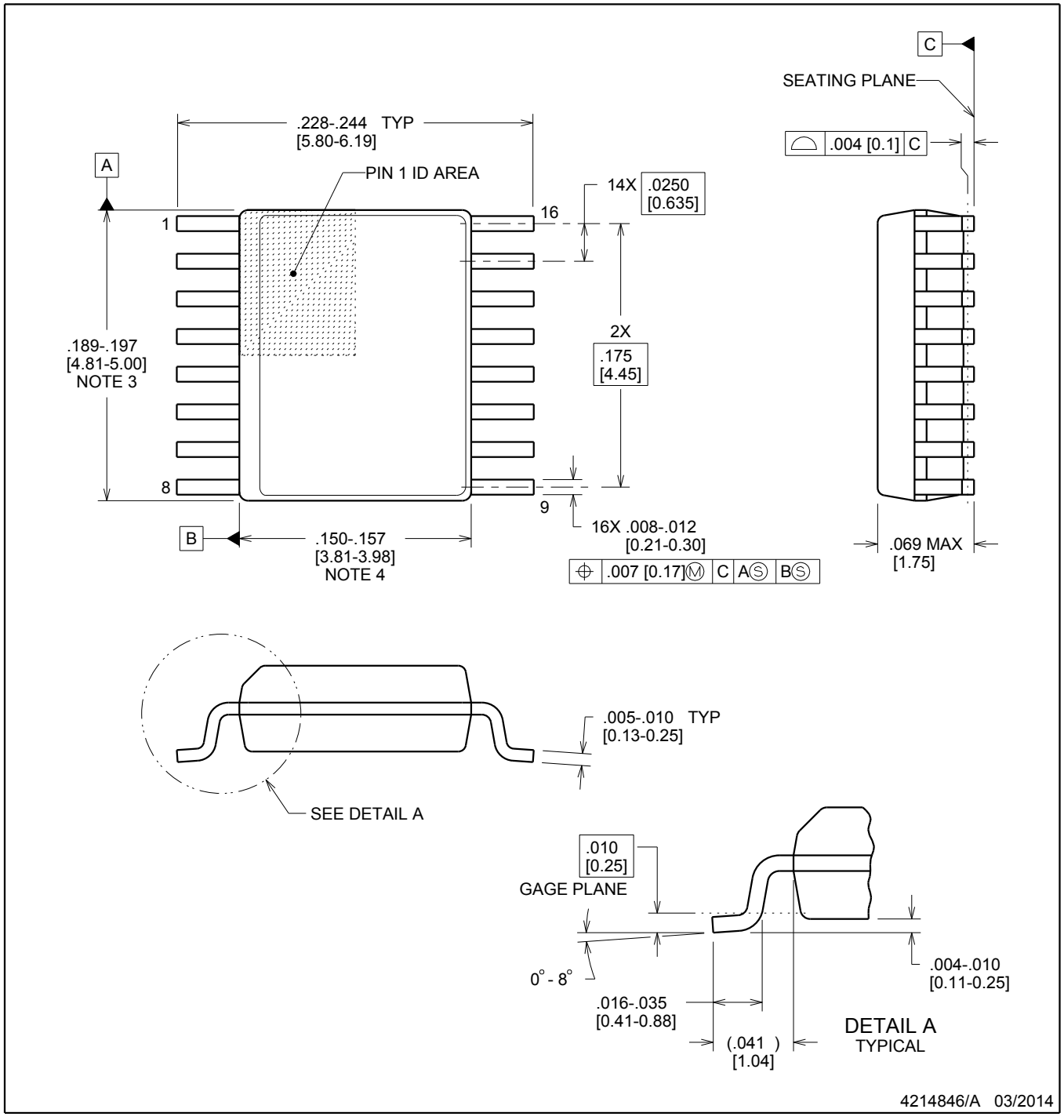


PACKAGE OUTLINE

DBQ0016A

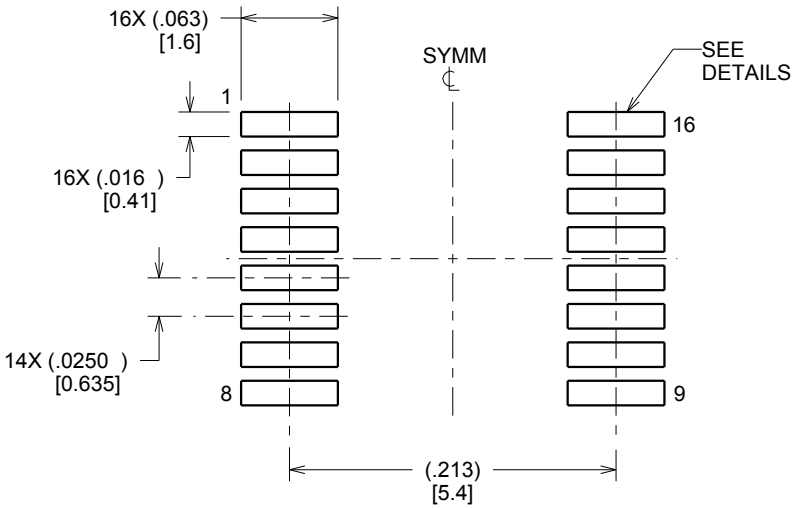
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

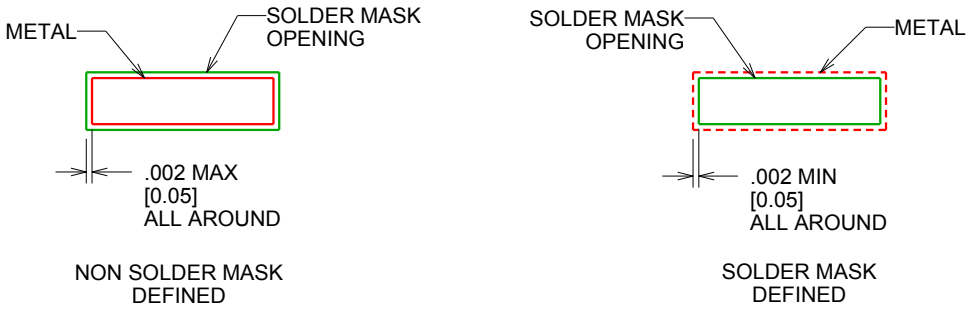


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

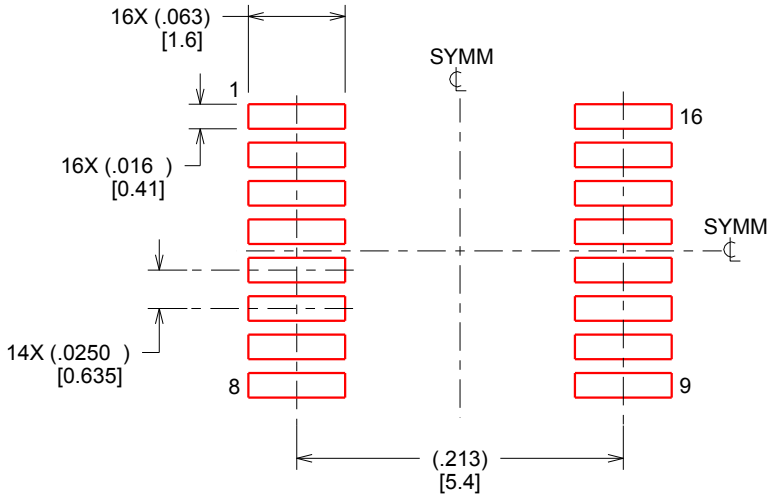
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

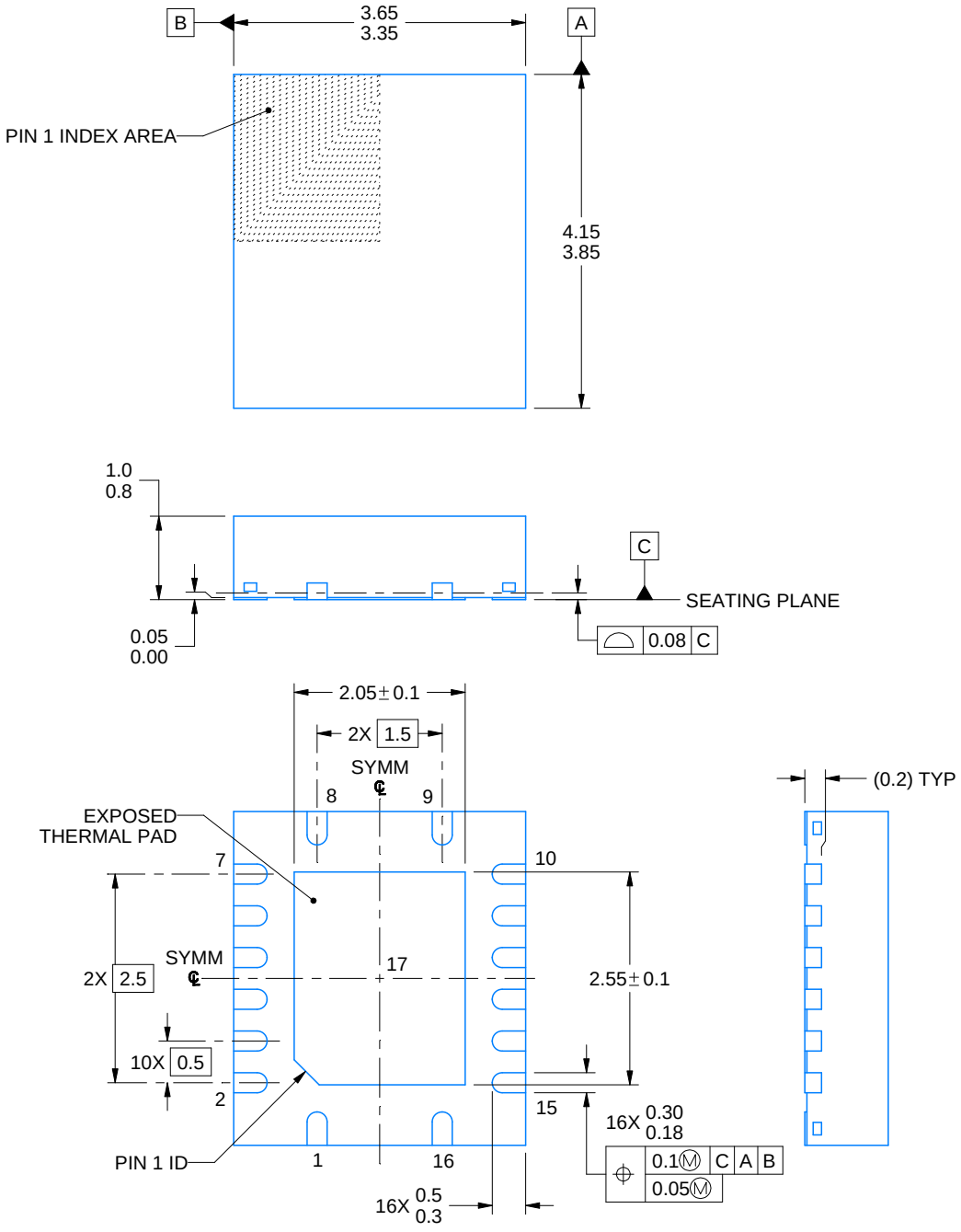
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY0016A

PACKAGE OUTLINE

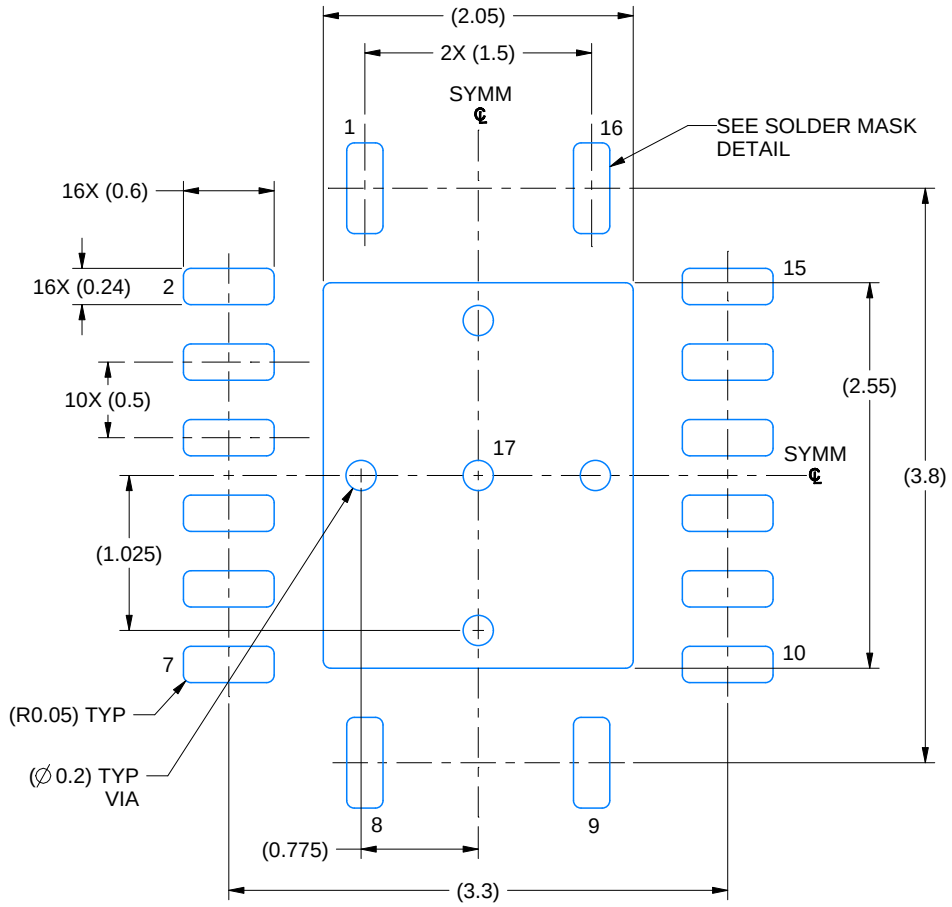
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

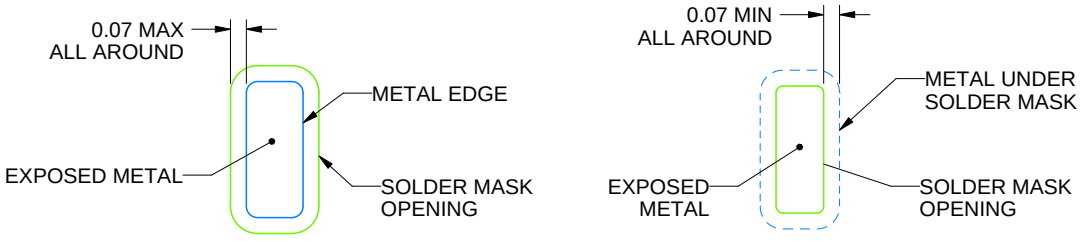


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

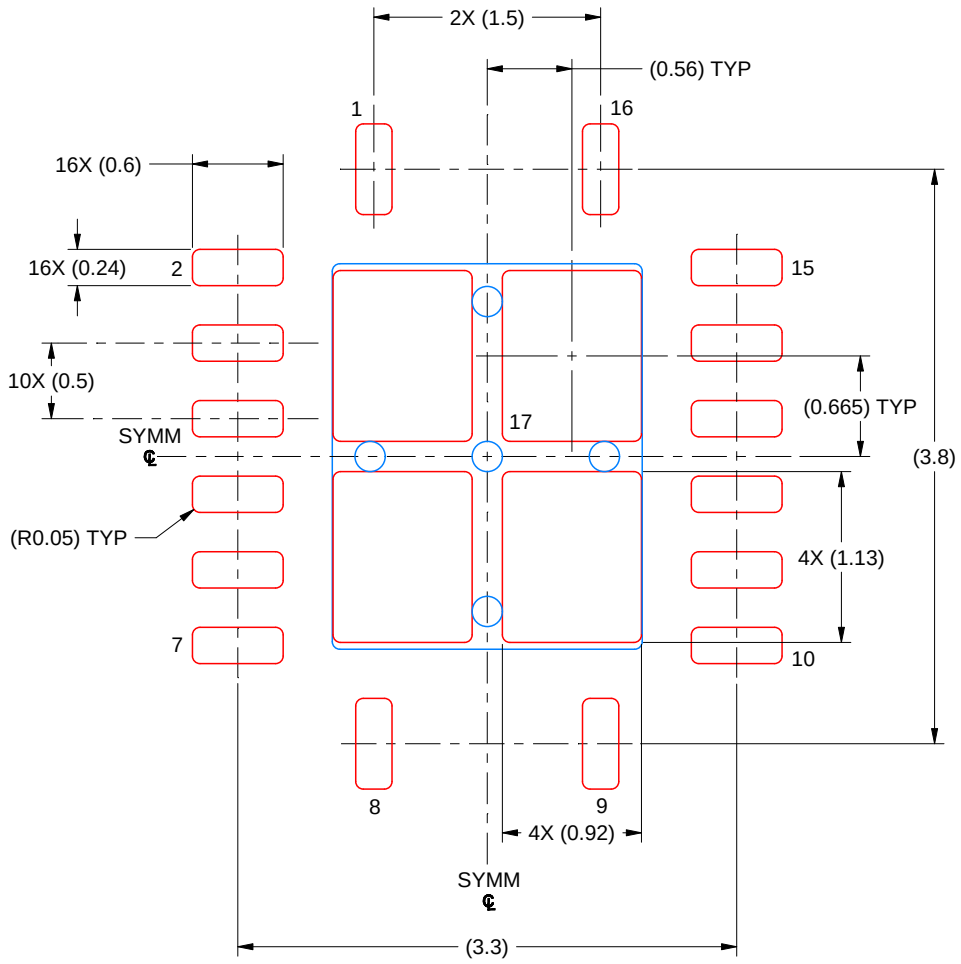


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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