

1:8 LVTTL TO M-LVDS REPEATER DUAL 1:4 LVTTL TO M-LVDS REPEATER

FEATURES

- **LVTTL Receiver and Eight Line Drivers Configured as an 8-Port M-LVDS Repeater – SN65MLVD128**
- **2 LVTTL Receivers and Eight Line Drivers Configured as Dual 4-Port M-LVDS Repeaters – SN65MLVD129**
- **Drivers Meet or Exceed the M-LVDS Standard (TIA/EIA-899)**
- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers for Data Rates (1) Up to 250 Mbps or Clock Frequencies Up to 125 MHz**
- **Power Up/Down Glitch Free**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**

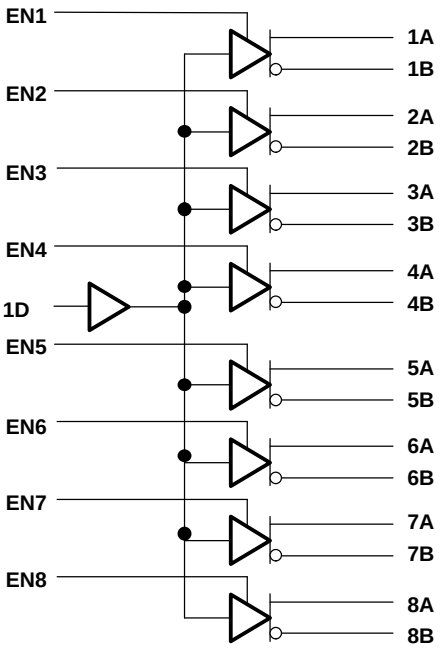
(1) The data rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

- **Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V**
- **Independent Enables for each Driver**
- **Output-to-Ouput Skew $t_{sk(o)} \leq 160$ ps Part-to-Part Skew $t_{sk(pp)} \leq 800$ ps**
- **Single 3.3-V Voltage Supply**
- **Bus Pin ESD Protection Exceeds 9 kV**
- **Packaged in 48-Pin TSSOP (DGG)**

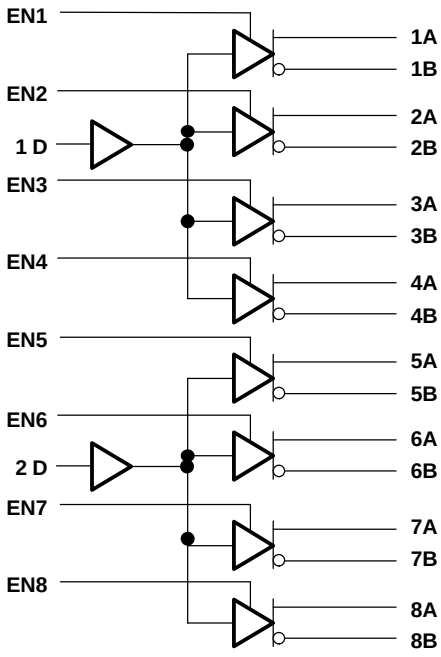
APPLICATIONS

- **AdvancedTCA™ (ATCA™) Clock Bus Driver**
- **Clock Distribution**
- **Data and Clock Repeating Over Backplanes and Cables**
- **Cellular Base Stations**
- **Central Office Switches**
- **Network Switches and Routers**

LOGIC DIAGRAM



SN65MLVD128



SN65MLVD129

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The SN65MLVD128 and SN65MLVD129 are LVTTL-to-M-LVDS translators/repeaters. Outputs comply with the M-LVDS standard (TIA/EIA-899) and are optimized for data rates up to 250 Mbps, and clock frequencies up to 125 MHz. The driver outputs have been designed to support multipoint buses presenting loads as low as 30 Ω and incorporates controlled transition times for backbone operation.

M-LVDS compliant devices allow for 32 nodes on a common bus, providing a high-speed replacement for RS-485 devices when lower common-mode voltage range and lower output signaling levels are acceptable. The SN65MLVD128 and SN65MLVD129 provide separate driver enables, allowing for independent control of each output signal.

Intended applications for these devices include transmission of clock signals from a central clock module, as well as translation and buffering of data or control signals for transmission through a controlled impedance backplane or cable.

ORDERING INFORMATION

PART NUMBER	INPUT/OUTPUT CHANNEL	PART MARKING	PACKAGE/CARRIER
SN65MLVD128DGG	1:8	MLVD128	48-Pin TSSOP/Tube
SM65MLVD128DGGR	1:8	MLVD128	48-Pin TSSOP/Tape and Reeled
SN65MLVD129DGG	Dual 1:4	MLVD129	48-Pin TSSOP/Tube
SM65MLVD129DGGR	Dual 1:4	MLVD129	48-Pin TSSOP/Tape and Reeled

PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
48-DGG	Low-K(2)	1114.6 mW	9.7 mW/°C	533.1 mW
48-DGG	High-K(3)	1824.5 mW	15.9 mW/°C	872.6 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

				SN65MLVD128, 129
V_{CC}	Supply voltage range(2)			–0.5 V to 4 V
V_I	Input voltage range	D, EN		–0.5 V to 4 V
V_O	Output voltage range	A or B		–1.8 V to 4 V
	Electrostatic discharge	Human Body Model(3)	A, B	±9 kV
			All pins	±4 kV
		Charged-Device Model(4)	All pins	±1500 V
		Machine Model(5)	All pins	200 V
	Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage (1)	2		V_{CC}	V
V_{IL}	Low-level input voltage (2)	0		0.8	V
	Voltage at any bus terminal (separate or common mode) V_A or V_B	–1.4		3.8	V
R_L	Differential load resistance	30		55	Ω
$1/t_{UI}$	Signaling rate			250	Mbps
	Clock frequency			125	MHz
T_A	Ambient temperature	–40		85	°C

(1) In accordance with the High-K thermal metric difinitions of EIA/JESD51-7.
(2) In accordance with the Low-K thermal metric difinitions of EIA/JESD51-3.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN (1)	TYP (2)	MAX	UNIT
I_{CC}	Supply current	Driver enabled	EN = V_{CC}, Input = V_{CC} or GND, R_L = 50 Ω		112	140	mA
			EN = V_{CC}, Input = V_{CC} or GND, R_L = No load			45	mA
		Driver disabled	EN = V_{CC}, Input = V_{CC} or GND, R_L = 50 Ω			7	mA
			EN = V_{CC}, Input = V_{CC} or GND, R_L = No load			7	mA
P_D	Device power dissipation		V_{CC} = 3.6 V, EN = V_{CC}, C_L = 15 pF, R_L = 50 Ω, Input 125 MHz 50 % duty cycle square wave, T_A = 85°C			529	mW

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
LVTTL (D, EN) INPUT SPECIFICATIONS						
$\|I_{IH}\|$	High-level input current	V_{IH} = 2 V or V_{CC}			10	µA
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND or 0.8 V			10	µA
C_i	Input capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V(3)		5		pF
M-LVDS (A, B) OUTPUT SPECIFICATIONS						
$\|V_{AB}\|$	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta\|V_{AB}\|$	Change in differential output voltage magnitude between logic states	See Figure 2	–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3			150	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output	See Figure 5	–0.2 V_{SS}			V
$\|I_{OS}\|$	Differential short-circuit output current magnitude	See Figure 4			24	mA
I_{OZ}	High-impedance state output current	–1.4 V ≤ (V_A or V_B) ≤ 3.8 V, Other output = 1.2 V	–20		20	µA
$I_{O(OFF)}$	Power-off output current	–1.4 V ≤ (V_A or V_B) ≤ 3.8 V, Other output = 1.2 V, 0 ≤ V_{CC}≤ 1.5 V	–20		20	µA
C_A orC_B	Output capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V, (3) Other input at 1.2 V, driver disabled		3		pF
C_{AB}	Differential output capacitance	V_I = 0.4 sin(30E6πt) V, (3) Driver disabled			2.5	pF
$C_{A/B}$	Output capacitance balance, (C_A/C_B)		0.99		1.01	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 5	1		3	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1		3	ns
t_r	Differential output signal rise time		1		2	ns
t_f	Differential output signal fall time		1		2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				100	ps
$t_{sk(o)}$	Output skew				160	ps
$t_{sk(bb)}$	Bank-to-bank skew(2)				100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				800	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	100 MHz clock input, All channels enabled		1	3	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter(4)	100 MHz clock input, All channels enabled			20	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	200 Mbps 2^{15}-1 PRBS input, All channels enabled		46	110	ps
t_{PZH}	Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output				7	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 6			7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output				7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(bb)}$, which only applies to the SN65MLVD129, is the magnitude of the difference between the t_{PLH} and t_{PHL} of two outputs of any bank.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Stimulus jitter has been subtracted from the numbers.

PARAMETER MEASUREMENT INFORMATION

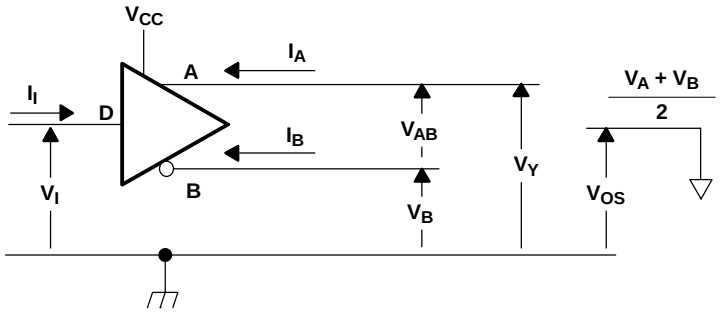
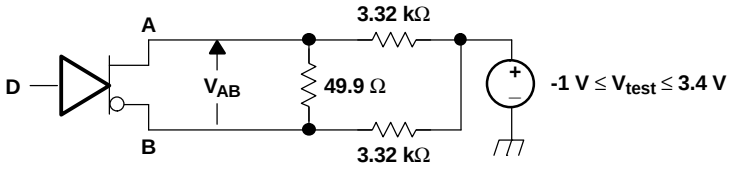
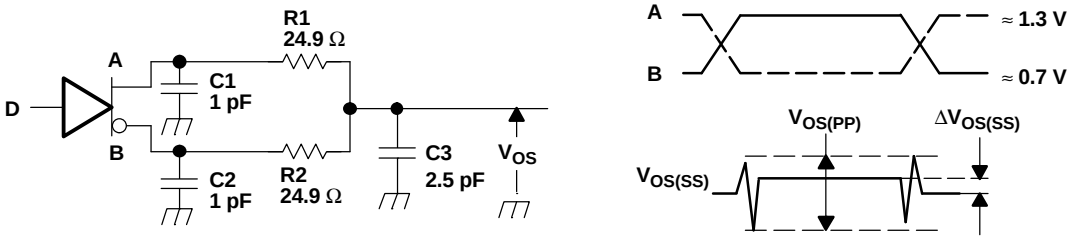


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

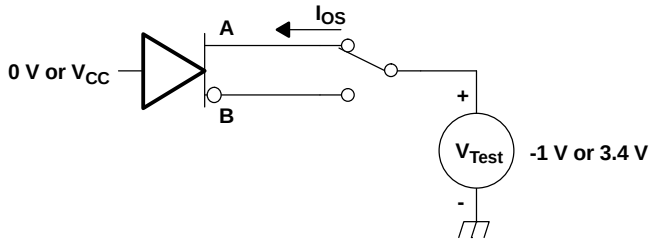
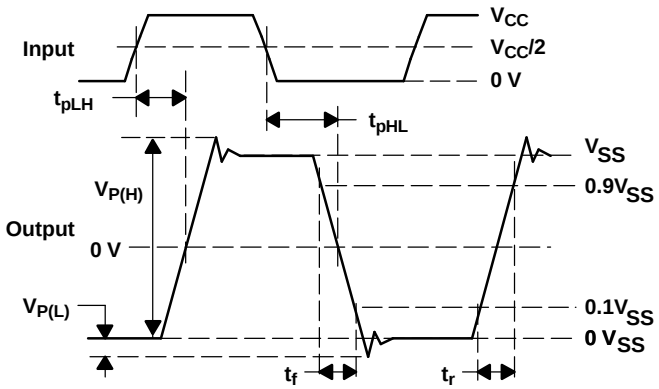


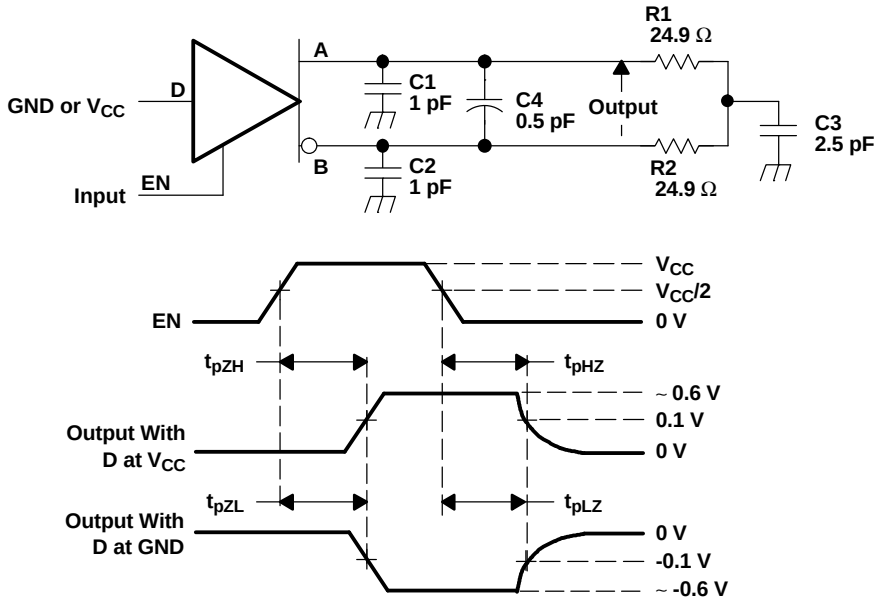
Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

B. C1, C2, C3, and C4 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

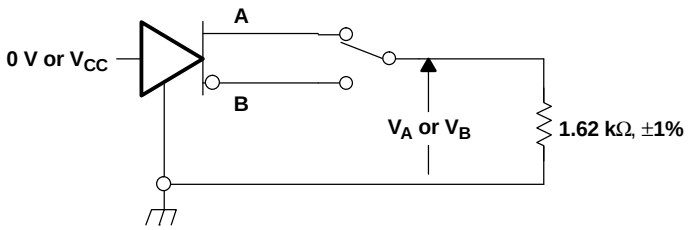
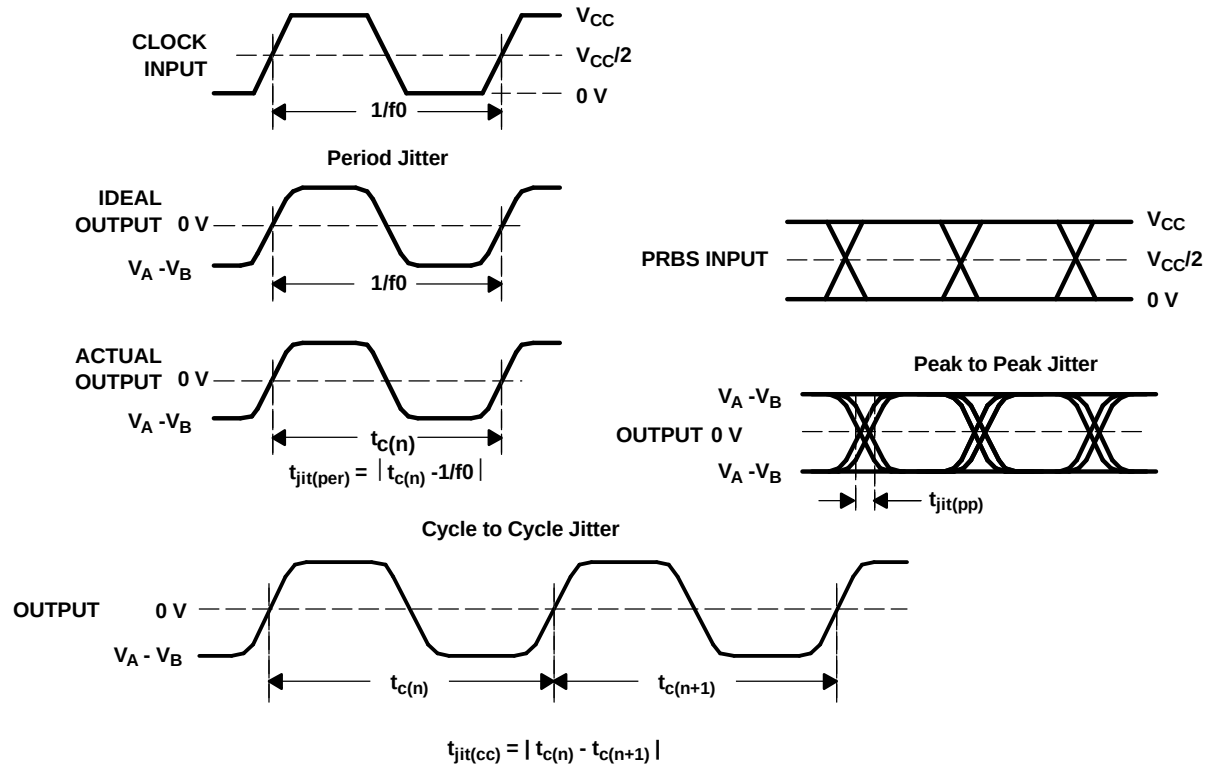


Figure 7. Driver Maximum Steady State Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



$t_{jit(cc)} = | t_{c(n)} - t_{c(n+1)} |$

A. All input pulses are supplied by an Agilent 8304A Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

C. Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 ±1% duty cycle clock input.

D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}-1 PRBS input.

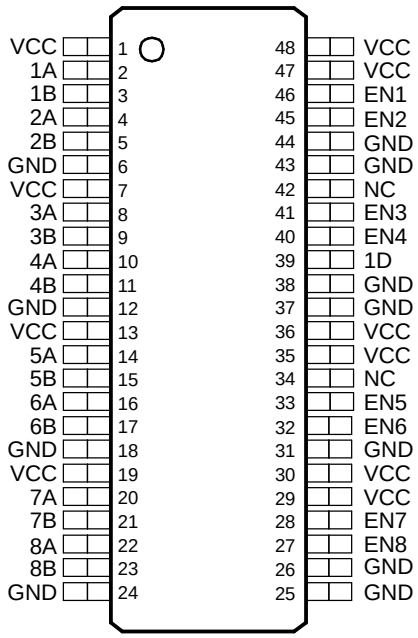
Figure 8. Driver Jitter Measurement Waveforms

Table 1. Terminal Functions

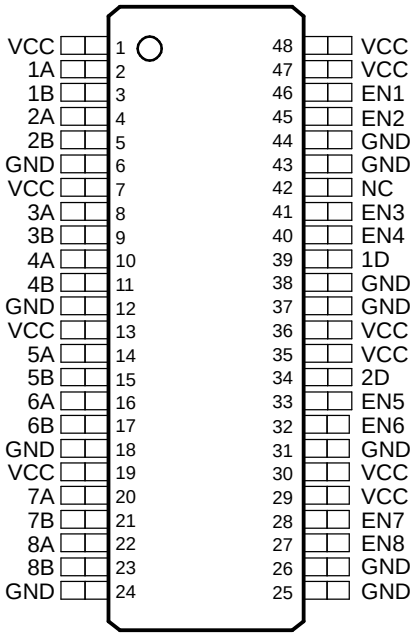
PIN		TYPE	DESCRIPTION
NAME	NO.		
SN65MLVD128			
1D	39	Input	Data inputs for drivers
EN1–EN8	27, 28, 32, 33, 40, 41, 45, 46	Input	Driver enable, active high, individual enables
1A–8A	2, 4, 8, 10, 14, 16, 20, 22	Output	M-LVDS bus noninverting output
1B–8B	3, 5, 9, 11, 15, 17, 21, 23	Output	M-LVDS bus inverting output
GND	6, 12, 18, 24, 25, 26, 31, 37, 38, 43, 44	Power	Circuit ground
V_{CC}	1, 7, 13, 19, 29, 30, 35, 36, 47, 48	Power	Supply voltage
NC	34, 42	N/A	Not connected
SN65MLVD129			
1D, 2D	39, 34	Input	Data inputs for drivers
EN1–EN8	27, 28, 32, 33,40, 41, 45, 46	Input	Driver enable, active high, individual enables
1A–8A	2, 4, 8, 10,14, 16, 20, 22	Output	M-LVDS bus noninverting output
1B–8B	3, 5, 9, 11,15, 17, 21, 23	Output	M-LVDS bus inverting output
GND	6, 12, 18, 24, 25, 26, 31, 37, 38, 43, 44	Power	Circuit ground
V_{CC}	1, 7, 13, 19, 29, 30, 35, 36, 47, 48	Power	Supply voltage
NC	42	N/A	Not connected

PIN ASSIGNMENTS

MLVD128DGG
48-TSSOP PACKAGE
(TOP VIEW)



MLVD129DGG
48-TSSOP PACKAGE
(TOP VIEW)



NC - No internal connection

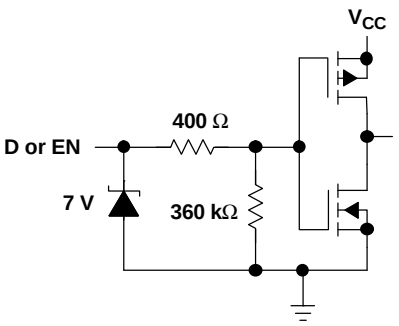
FUNCTION TABLE

MLVD128 / MLVD129 (1)			
INPUT	ENABLE	OUTPUTS	
D	EN	A	B
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

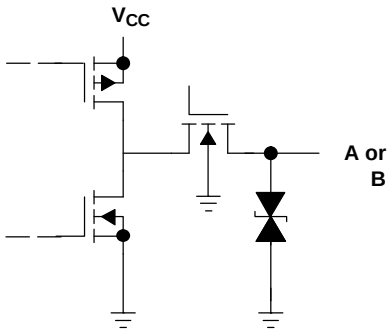
(1) H = high level, L = low level, Z = high impedance, X = Don't care, OPEN = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

DRIVER INPUT AND DRIVER ENABLE



DRIVER OUTPUT



TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT vs INPUT FREQUENCY

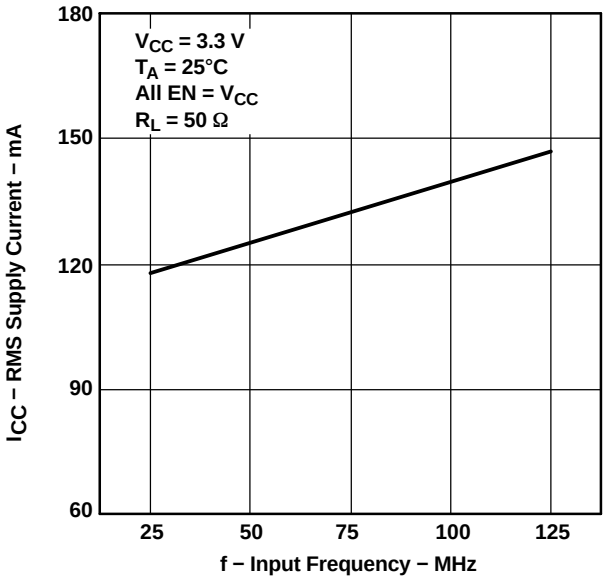


Figure 9.

RMS SUPPLY CURRENT vs FREE-AIR TEMPERATURE

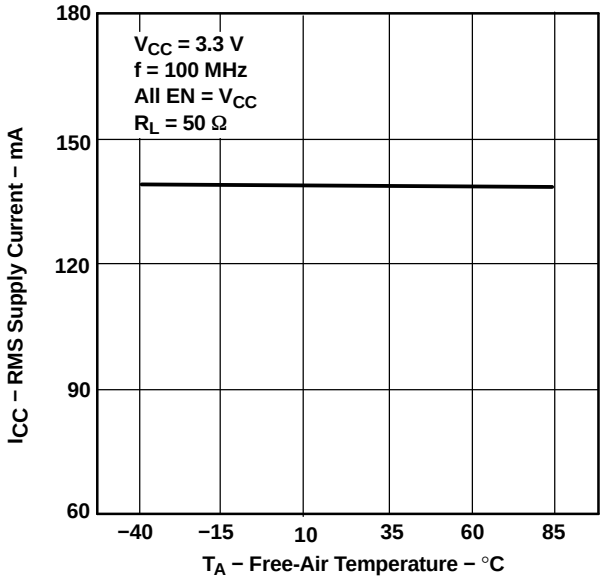


Figure 10.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE MAGNITUDE
vs
INPUT FREQUENCY

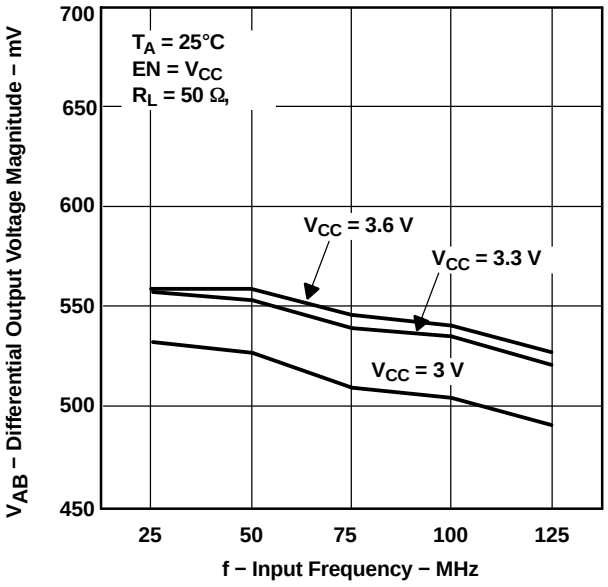


Figure 11.

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

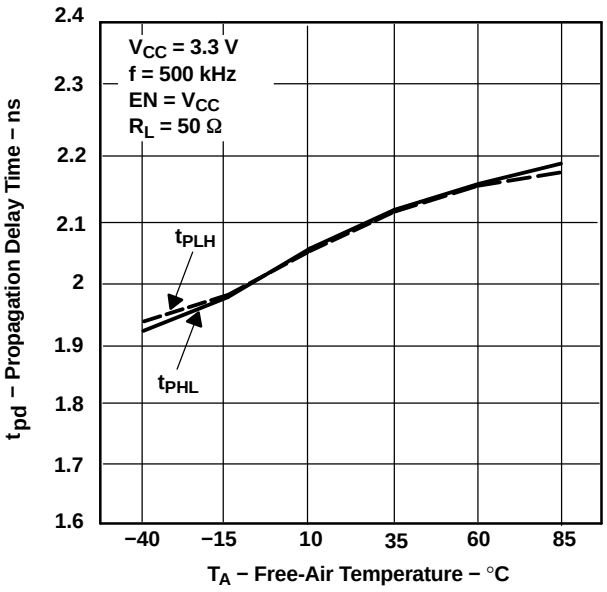


Figure 12.

TRANSITION TIME
vs
FREE-AIR TEMPERATURE

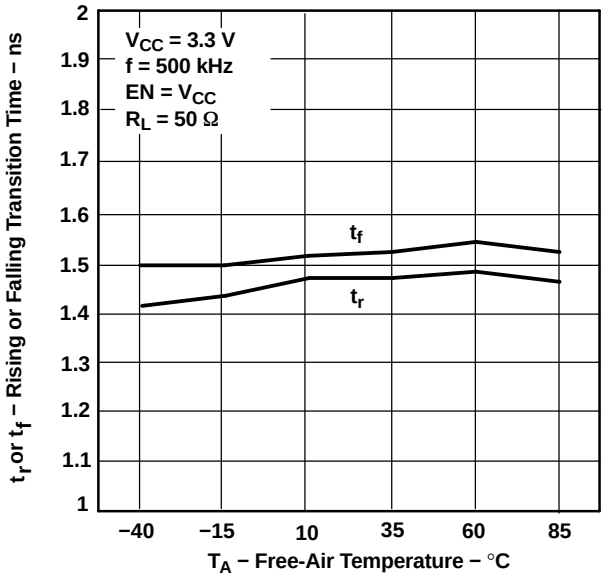


Figure 13.

PEAK-TO-PEAK JITTER
vs
DATA RATE

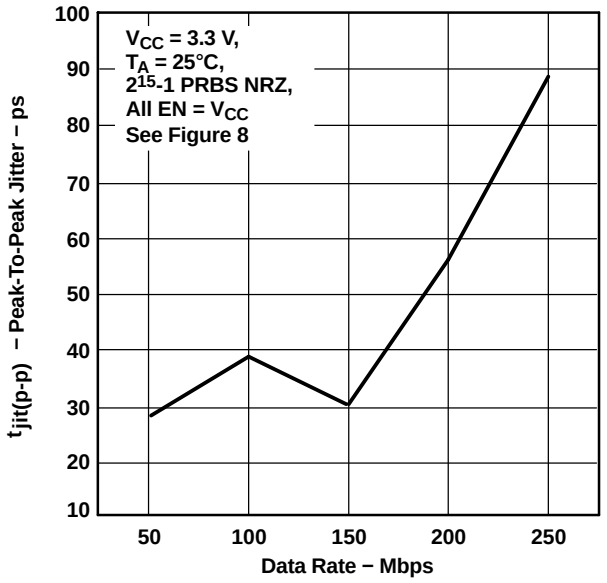


Figure 14.

TYPICAL CHARACTERISTICS (continued)

PERIOD JITTER
vs
CLOCK FREQUENCY

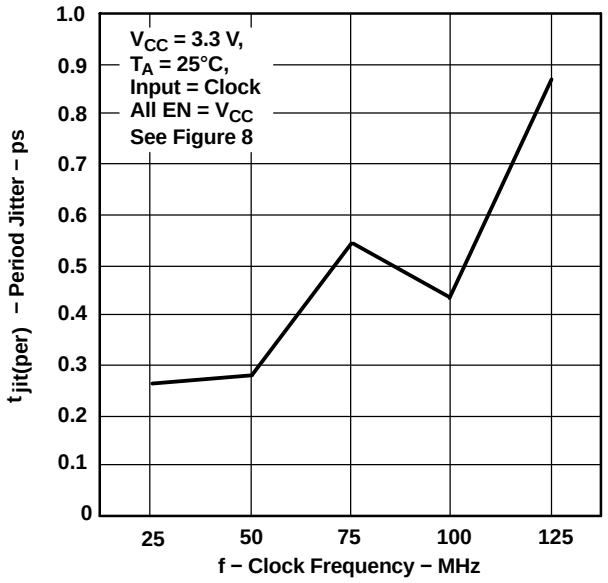


Figure 15.

CYCLE-TO-CYCLE JITTER
vs
CLOCK FREQUENCY

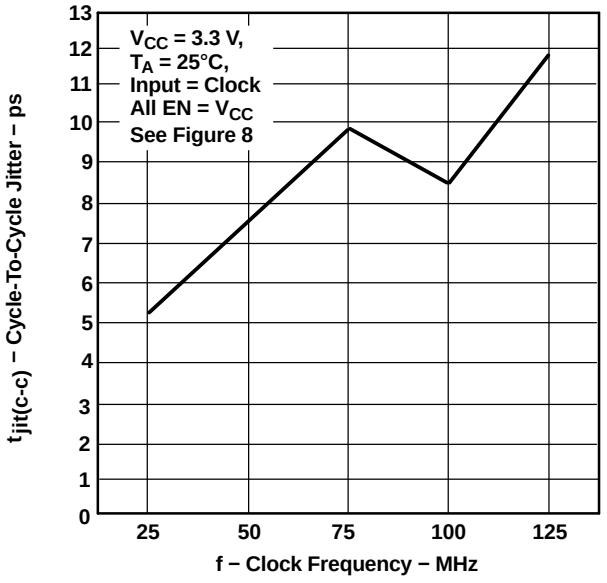
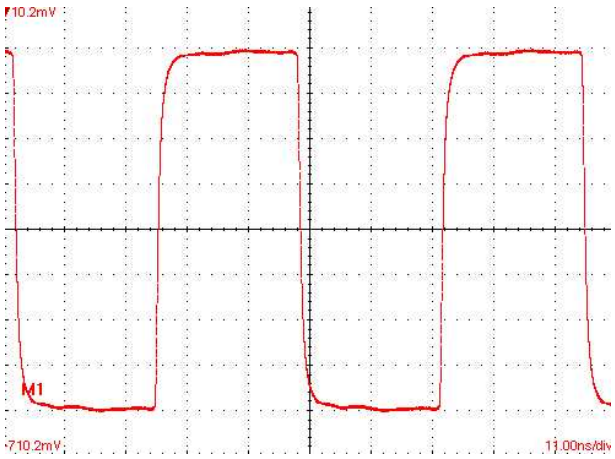


Figure 16.

APPLICATION INFORMATION

CLOCK DISTRIBUTION

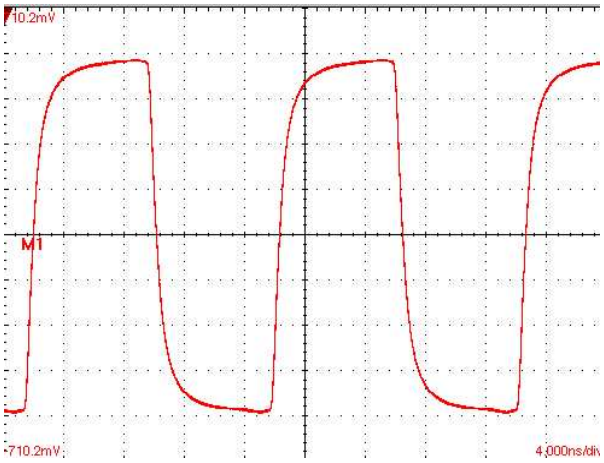
SN65MLVD128 Output
Input Source: 19.6608 MHz Clock With 50%
Duty Cycle, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 2.5 pF



Output Duty cycle = 49.97%.
Vertical scale = 142 mV/div
Horizontal scale = 11 ns/div

Figure 17.

SN65MLVD128 Output
Input Source: 61.44 MHz Clock With 50%
Duty Cycle, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 2.5 pF

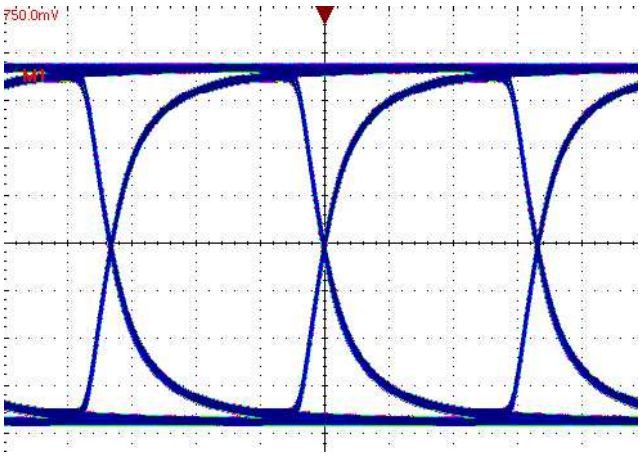


Output duty cycle = 50.01%.
Vertical scale = 142 mV/div
Horizontal scale = 4 ns/div

Figure 18.

DATA DISTRIBUTION

SN65MLVD128 Output
Input Source: 250 Mbps, 2^{15}-1 PRBS,
V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 2.5 pF



Vertical scale = 150 mV/div
Horizontal scale = 1.21 ns/div

Figure 19.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65MLVD128DGGG4	Last Time Buy	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MLVD128
SN65MLVD128DGGG4.B	Last Time Buy	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MLVD128

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

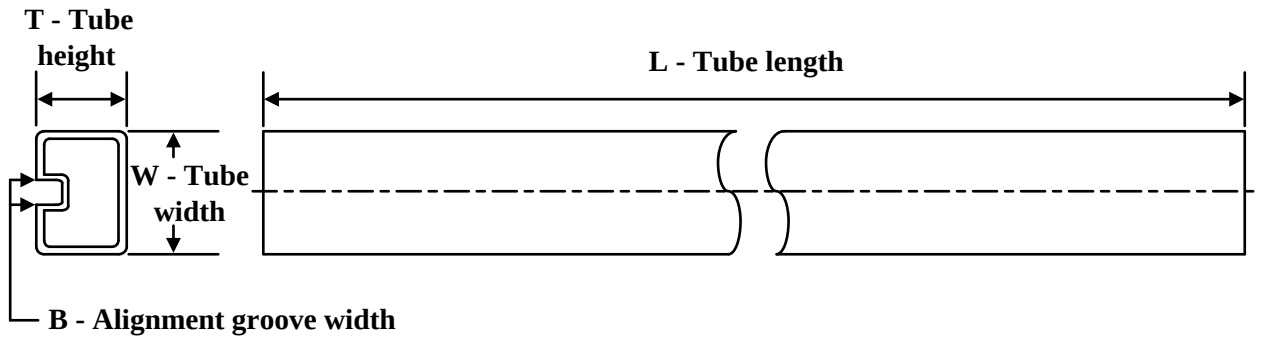
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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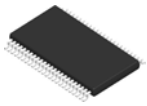
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65MLVD128DGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN65MLVD128DGGG4.B	DGG	TSSOP	48	40	530	11.89	3600	4.9

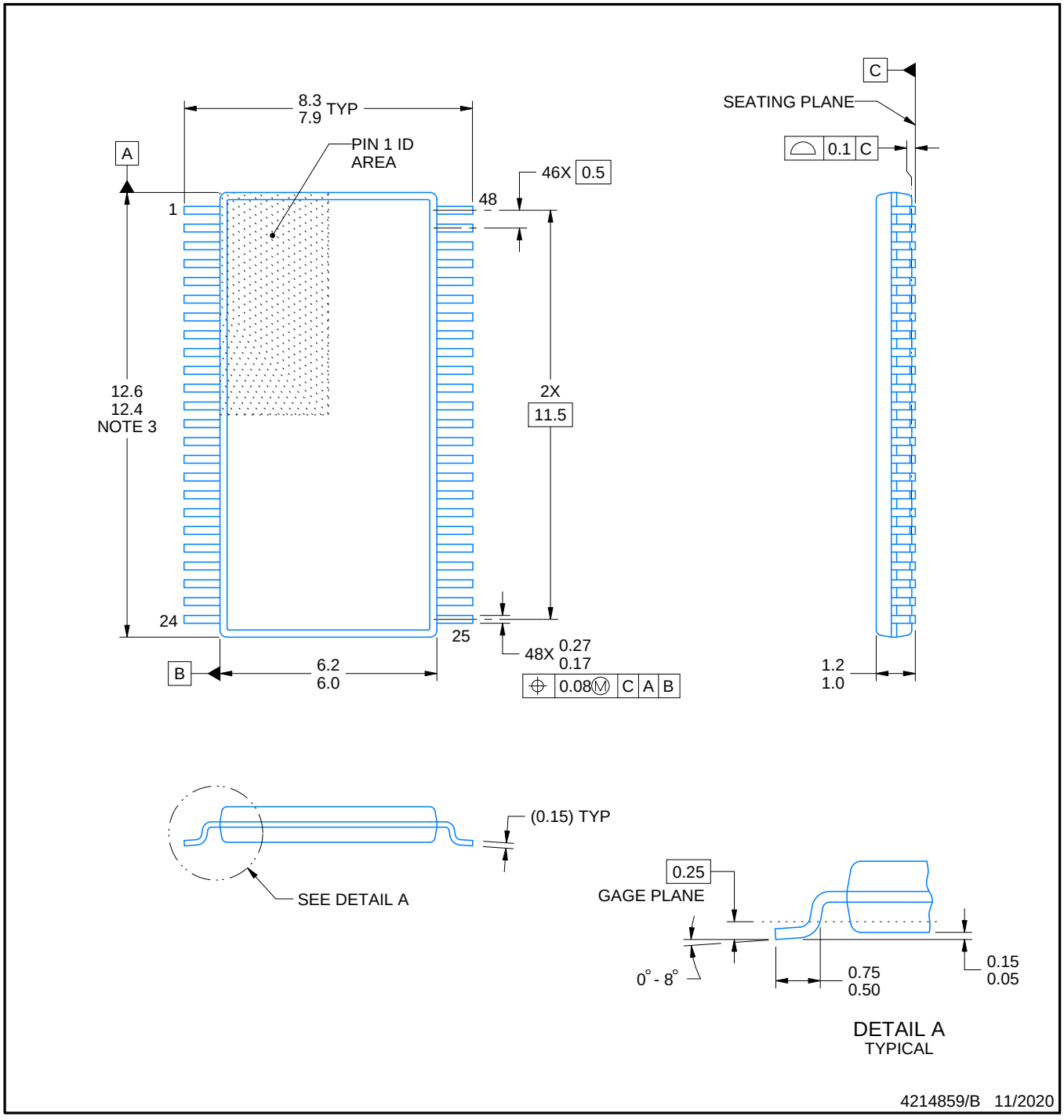


PACKAGE OUTLINE

DGG0048A

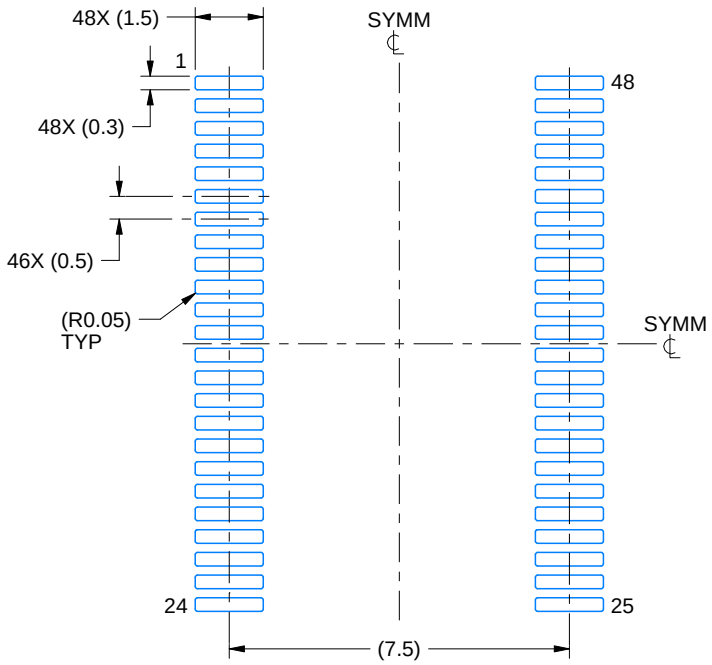
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

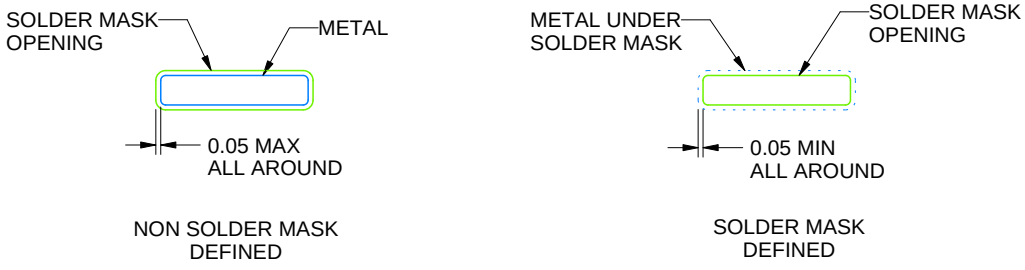


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

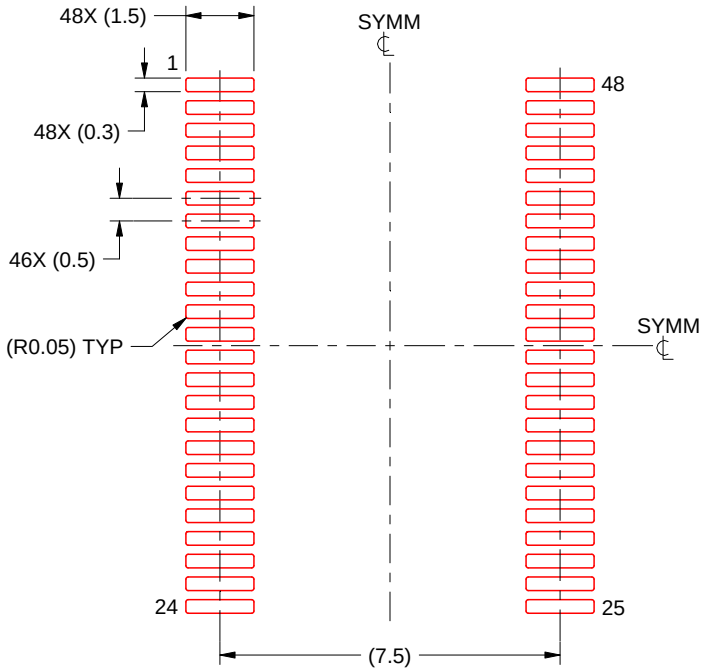


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

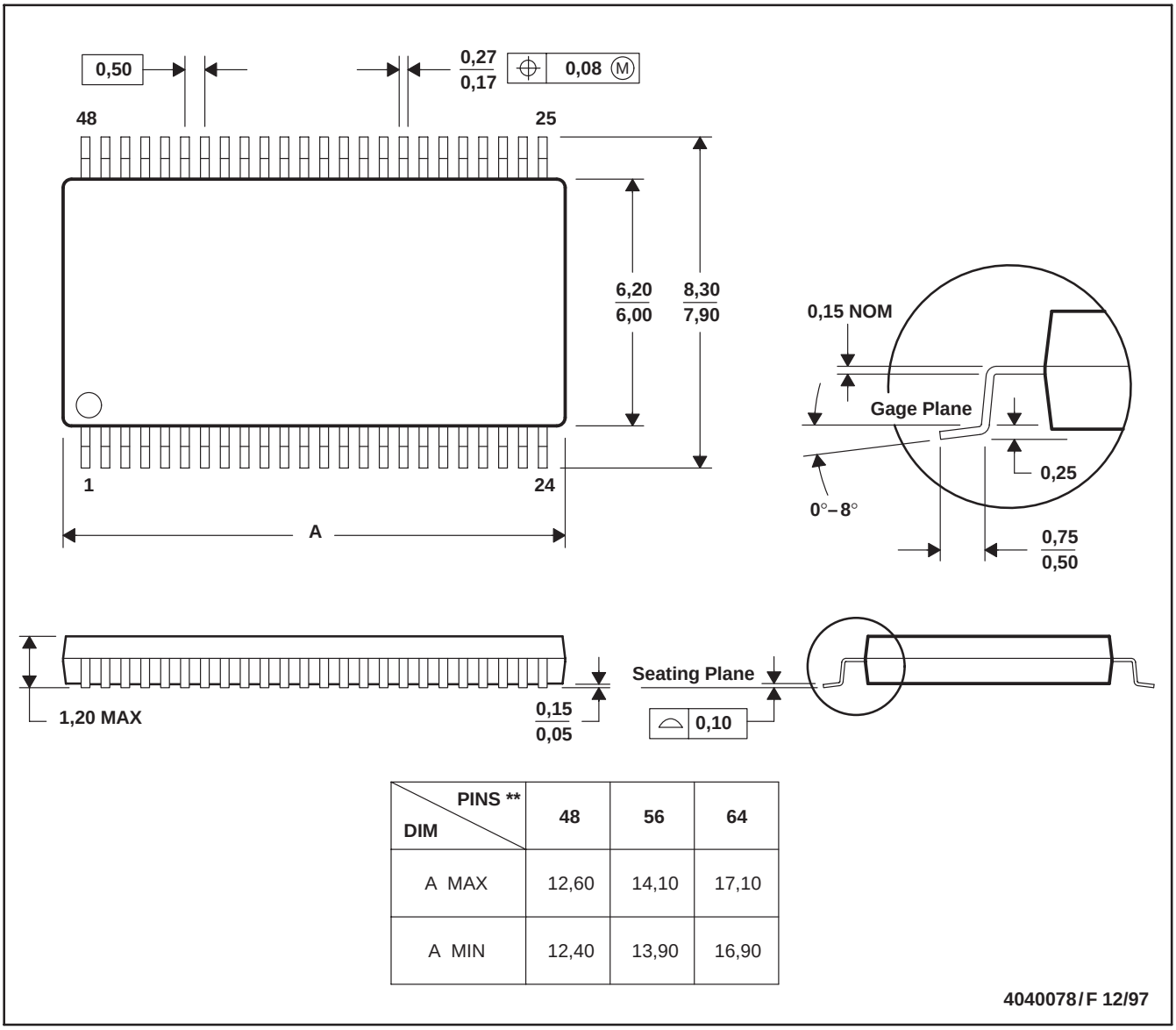
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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