INA826 Precision, 200-µA Supply Current, 3-V to 36-V Supply Instrumentation Amplifier With Rail-to-Rail Output

1 Features

- Input common-mode range: Includes V–
- Common-mode rejection:
  - 104 dB, min (G = 10)
  - 100 dB, min at 5 kHz (G = 10)
- Power-supply rejection: 100 dB, min (G = 1)
- Low offset voltage: 150 µV, max
- Gain drift: 1 ppm/°C (G = 1), 35 ppm/°C (G > 1)
- Noise: 18 nV/√Hz, G ≥ 100
- Bandwidth: 1 MHz (G = 1), 60 kHz (G = 100)
- Inputs protected up to ±40 V
- Rail-to-rail output
- Supply current: 200 µA
- Supply range:
  - Single supply: 3 V to 36 V
  - Dual supply: ±1.5 V to ±18 V
- Specified temperature range: –40°C to +125°C
- Packages: 8-pin VSSOP, SOIC, and WSON

2 Applications

- Analog input module
- Flow transmitter
- Battery test
- LCD test
- Electrocardiogram (ECG)
- Surgical equipment
- Process analytics (pH, gas, concentration, force and humidity)
- Circuit breaker (ACB, MCCB, VCB)

3 Description

The INA826 is a cost-effective instrumentation amplifier that offers extremely low power consumption and operates over a very wide single-supply or dual-supply range. A single external resistor sets any gain from 1 to 1000. The device offers excellent stability over temperature, even at G > 1, as a result of the low gain drift of only 35 ppm/°C (maximum).

The INA826 is optimized to provide excellent common-mode rejection ratio of over 100 dB (G = 10) over frequencies up to 5 kHz. At G = 1, the common-mode rejection ratio exceeds 84 dB across the full input common-mode range, from the negative supply all the way up to 1 V of the positive supply. Using a rail-to-rail output, the INA826 is a great choice for low-voltage operation from a 3-V single supply, as well as dual supplies up to ±18 V.

Additional circuitry protects the inputs against overvoltage of up to ±40 V beyond the power supplies by limiting the input currents to less than 8 mA.

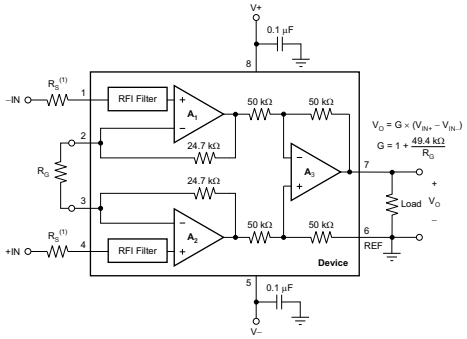
The INA826 is available in 8-pin SOIC, VSSOP, and tiny 3-mm × 3-mm WSON surface-mount packages. All versions are specified for the –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA826	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	3.00 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

General-Purpose Instrumentation Amplifier



(1) This resistor is optional if the input voltage stays above [(V–) – 2 V] or if the signal source current drive capability is limited to less than 3.5 mA; see the *Input Protection* section for more details.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2016) to Revision G — **Page**

- Changed Figure 58, *INA826 Simplified Circuit Diagram* ... 19
- Added last bullet regarding new DRG package to *Layout Guidelines* section ... 33
- Changed Figure 73, *INA826 Example Layout* ... 34

Changes from Revision E (April 2013) to Revision F — **Page**

- Added *Device Information*, *ESD Ratings*, *Recommended Operating Conditions* tables, and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Added TI Design ... 1
- Changed 2.7-V to 3-V in document title ... 1
- Changed MSOP to VSSOP, SO to SOIC, and DRG to WSON throughout document ... 1
- Changed *Supply Range* Features bullet minimum voltage levels ... 1
- Changed *Packages* Features bullet ... 1
- Changed page 1 graphic ... 1
- Changed *Description* section for minor rewording, renaming of packages , and changing single supply voltage value from 2.7 V to 3 V ... 1
- Deleted DGK Package*Package/Ordering Information* table ... 4
- Changed *Temperature* parameter symbols in *Absolute Maximum Ratings* table ... 5
- Changed Input, *Differential impedance* and *Common-mode impedance* parameter symbols in *Electrical Characteristics* table ... 6
- Changed Input, V_{CM} parameter test conditions in *Electrical Characteristics* table ... 6
- Deleted Gain, *Range of gain parameter* symbol from *Electrical Characteristics* table ... 7
- Changed Power Supply, V_S parameter minimum specifications, and moved to *Recommended Operating Conditions* table ... 7
- Changed V_S voltage to 3.0 V and red V_{REF} trace to 1.5 V in Figure 9 and Figure 10 ... 9

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- Changed V_S voltage level to 3.0 V in Figure 29 12
- Changed blue V_S trace value to 3.0 V in Figure 36 13
- Changed 2.7 V to 3 V and 1.35 V to 1.5 V in *Operating Voltage* section 24
- Changed TINA-TI simulation circuit links in *Using TINA-TI SPICE-Based Analog Simulation Program with the INA826* section 29

Changes from Revision D (March 2013) to Revision E **Page**

- Deleted package marking column from Package/Ordering Information table 4

Changes from Revision C (March 2012) to Revision D **Page**

- Changed Input voltage range parameter specification value in *Absolute Maximum Ratings* table 5

Changes from Revision B (December 2011) to Revision C **Page**

- Changed product status from Mixed Status to Production Data 1
- Deleted gray shading and footnote 2 from Package/Ordering Information table 4
- Changed DFN-8 package to production data 4

Changes from Revision A (September 2011) to Revision B **Page**

- Deleted gray from SO-8 row in Package/Ordering Information 4

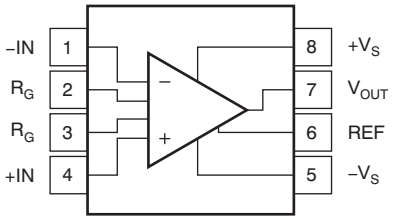
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5 Device Comparison Table

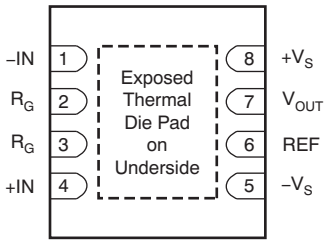
DEVICE	DESCRIPTION
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion
PGA112	Precision programmable gain op amp with SPI

6 Pin Configuration and Functions

DGK and D Package
8-Pin SOIC, VSSOP
Top View



DRG Package
8-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOIC, VSSOP	WSON		
–IN	1	1	I	Negative (inverting) input
+IN	4	4	I	Positive (noninverting) input
REF	6	6	I	Reference input. This pin must be driven by low impedance.
R_G	2	2	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
	3	3		
V_{OUT}	7	7	O	Output
$–V_S$	5	5	—	Negative supply
$+V_S$	8	8	—	Positive supply
Thermal pad	—	—	—	Exposed thermal die pad is internally connected to $–V_S$. Connect externally to $–V_S$ or leave floating.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–20	20	V
Signal input pins	Voltage	$(-V_S) - 40$	$(+V_S) + 40$	V
	REF pin	–20	+20	
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		175	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single-supply	3		36	V
	Dual-supply	±1.5		±18	
Specified temperature, T_A		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA826			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.4	215.4	50.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.4	66.3	60.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	97.8	25.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	10.5	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.1	96.1	25.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1)	RTI			40	150	µV
		vs temperature, T_A = –40°C to +125°C			0.4	2	µV/°C
V_{OSO}	Output stage offset voltage(1)	RTI			200	700	µV
		vs temperature, T_A = –40°C to +125°C			2	10	µV/°C
PSRR	Powersupply rejection ratio	G = 1, RTI		100	124		dB
		G = 10, RTI		115	130		
		G = 100, RTI		120	140		
		G = 1000, RTI		120	140		
z_{id}	Differential impedance				20 || 1		GΩ || pF
z_{ic}	Common-mode impedance				10 || 5		GΩ || pF
	RFI filter, –3-dB frequency				20		MHz
V_{CM}	Operating input range(2)			V–		(V+) – 1	V
		V_S = ±1.5 V to ±18 V T_A = –40°C to +125°C		See Figure 41 to Figure 44			
	Input overvoltage range	T_A = –40°C to +125°C				±40	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84	95		dB
			G = 10, V_{CM} = (V–) to (V+) – 1 V	104	115		
			G = 100, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1, V_{CM} = (V–) to (V+) – 1 V, T_A = –40°C to +125°C	80			
		At 5 kHz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84			
			G = 10, V_{CM} = (V–) to (V+) – 1 V	100			
			G = 100, V_{CM} = (V–) to (V+) – 1 V	105			
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	105			
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			35	65	nA
		T_A = –40°C to +125°C				95	
I_{OS}	Input offset current	V_{CM} = V_S / 2			0.7	5	nA
		T_A = –40°C to +125°C				10	
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise(3)	f = 1 kHz, G = 100, R_S = 0 Ω			18	20	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.52		$µV_{PP}$
e_{NO}	Output stage voltage noise(3)	f = 1 kHz, G = 1, R_S = 0 Ω			110	115	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 1, R_S = 0 Ω			3.3		$µV_{PP}$
I_n	Noise current	f = 1 kHz			100		fA/√Hz
		f_B = 0.1 Hz to 10 Hz			5		pA_{PP}

(1) Total offset, referred-to-input (RTI): V_{OS} = (V_{OSI}) + (V_{OSO} / G).
(2) Input voltage range of the INA826 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves Figure 9 through Figure 16 and Figure 41 through Figure 44 for more information.
(3)

$$\text{Total RTI voltage noise} = \sqrt{(e_{NI})^2 + \left(\frac{e_{NO}}{G}\right)^2}.$$

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
G	Gain equation				$1 + \left(\frac{49.4\ k\Omega}{R_G}\right)$		V/V
	Range of gain			1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V			±0.003%	±0.015%	
		G = 10, V_O = ±10 V			±0.03%	±0.15%	
		G = 100, V_O = ±10 V			±0.04%	±0.15%	
		G = 1000, V_O = ±10 V			±0.04%	±0.15%	
	Gain vs temperature(4)	G = 1, T_A = –40°C to +125°C			±0.1	±1	ppm/°C
		G > 1, T_A = –40°C to +125°C			±10	±35	
	Gain nonlinearity	G = 1 to 100, V_O = –10 V to +10 V			1	5	ppm
		G = 1000, V_O = –10 V to +10 V			5	20	
OUTPUT							
	Voltage swing	R_L = 10 kΩ		(V–) + 0.1		(V+) – 0.15	V
	Load capacitance stability				1000		pF
Z_O	Open-loop output impedance				See Figure 56		
I_{SC}	Short-circuit current	Continuous to V_S / 2			±16		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1		MHz
		G = 10			500		kHz
		G = 100			60		
		G = 1000			6		
SR	Slew rate	G = 1, V_O = ±14.5 V			1		V/µs
		G = 100, V_O = ±14.5 V			1		
t_S	Settling time	0.01%	G = 1, V_{STEP} = 10 V		12		µs
			G = 10, V_{STEP} = 10 V		12		
			G = 100, V_{STEP} = 10 V		24		
			G = 1000, V_{STEP} = 10 V		224		
		0.001%	G = 1, V_{STEP} = 10 V		14		
			G = 10, V_{STEP} = 10 V		14		
			G = 100, V_{STEP} = 10 V		31		
			G = 1000, V_{STEP} = 10 V		278		
REFERENCE INPUT							
R_{IN}	Input impedance				100		kΩ
	Voltage range			(V–)		(V+)	V
	Gain to output				1		V/V
	Reference gain error				0.01%		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			200	250	µA
		vs temperature, T_A = –40°C to +125°C			250	300	

(4) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

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7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

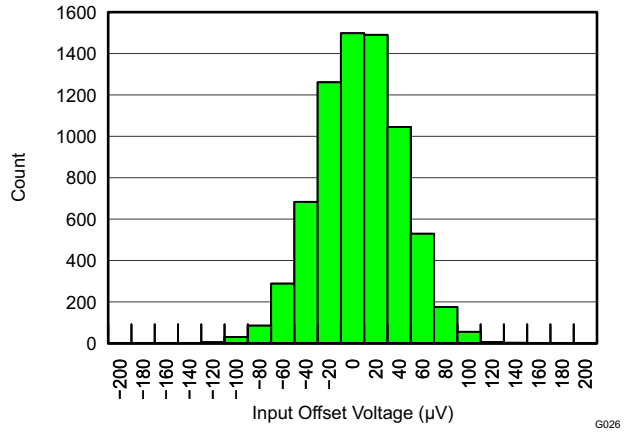


Figure 1. Typical Distribution of Input Offset Voltage

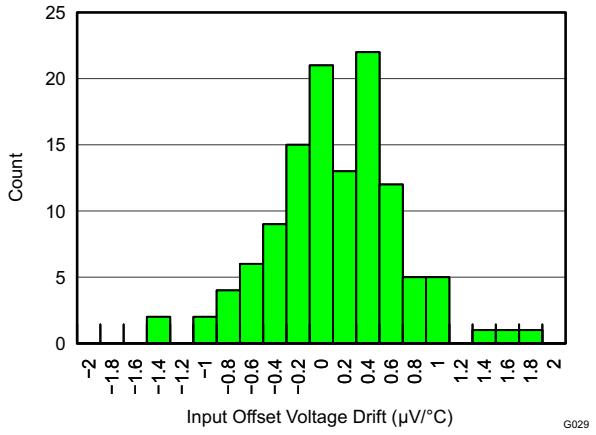


Figure 2. Typical Distribution of Input Offset Voltage Drift

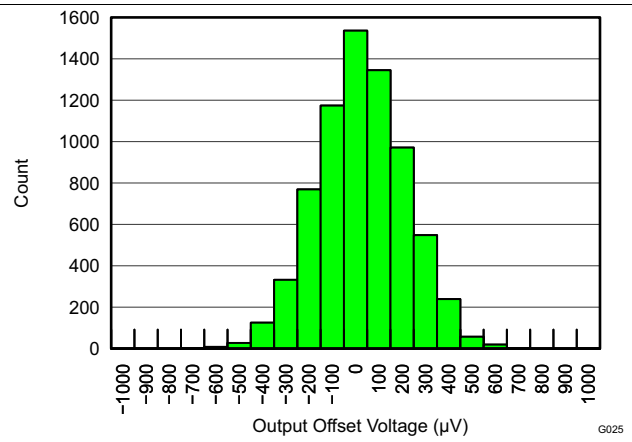


Figure 3. Typical Distribution of Output Offset Voltage

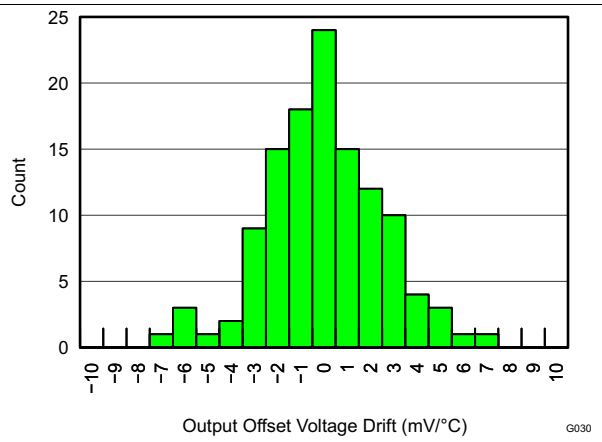


Figure 4. Typical Distribution of Output Offset Voltage Drift

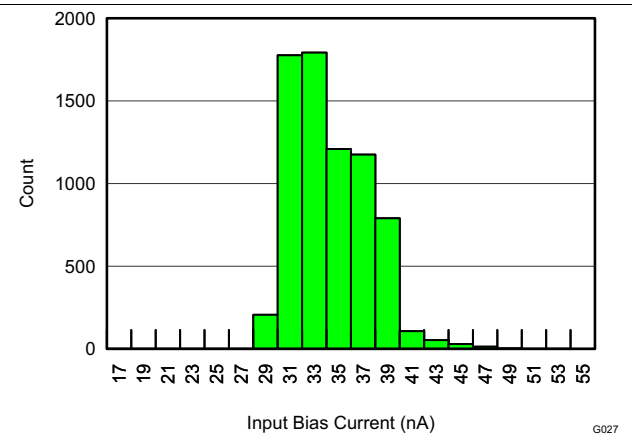


Figure 5. Typical Distribution of Input Bias Current

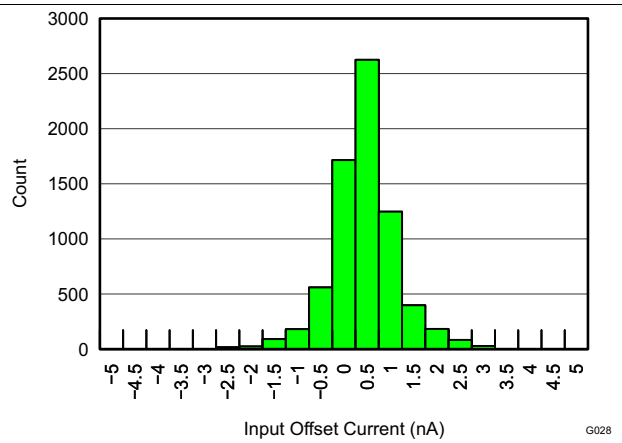
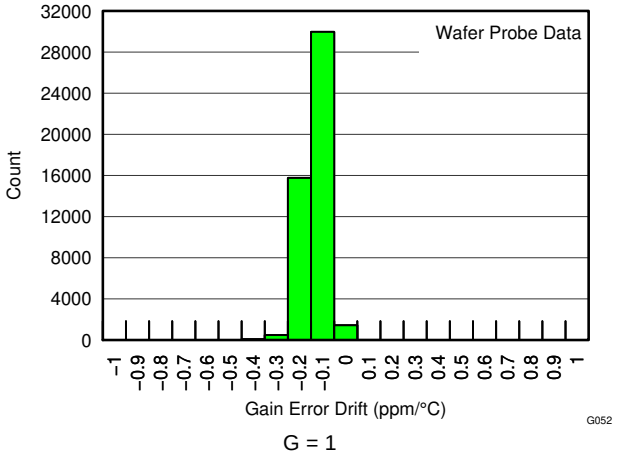


Figure 6. Typical Distribution of Input Offset Current

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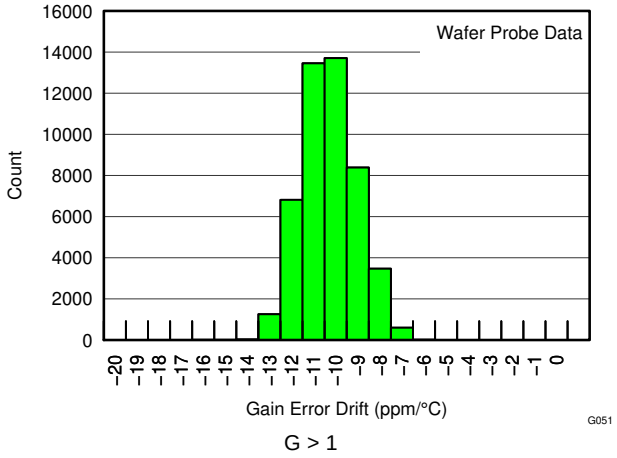
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



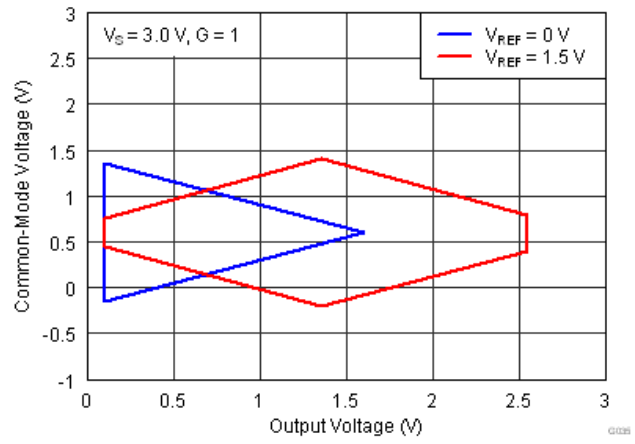
G = 1

Figure 7. Typical Gain Error Drift Distribution



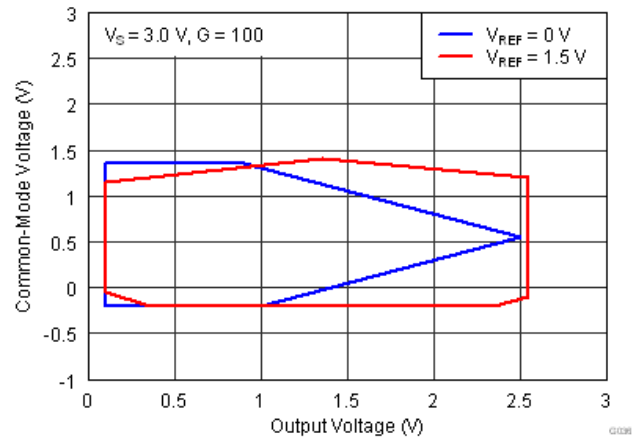
G > 1

Figure 8. Typical Gain Error Drift Distribution



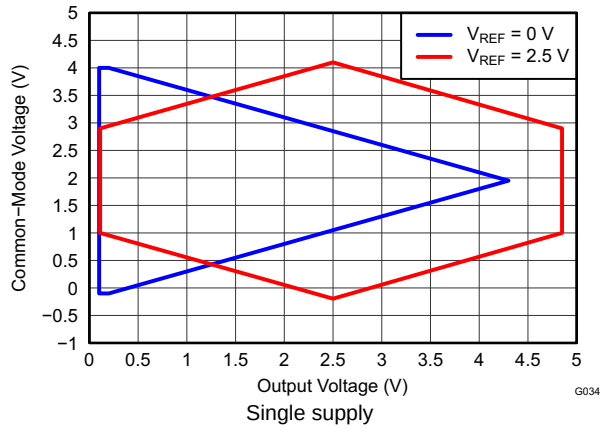
Single supply

Figure 9. Input Common-Mode Voltage vs Output Voltage



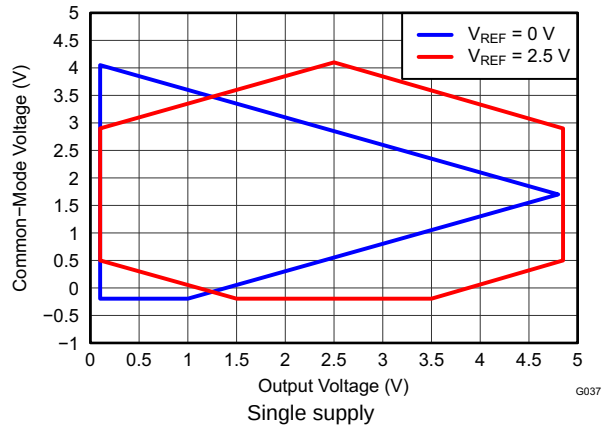
Single supply

Figure 10. Input Common-Mode Voltage vs Output Voltage



Single supply

Figure 11. Input Common-Mode Voltage vs Output Voltage



Single supply

Figure 12. Input Common-Mode Voltage vs Output Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

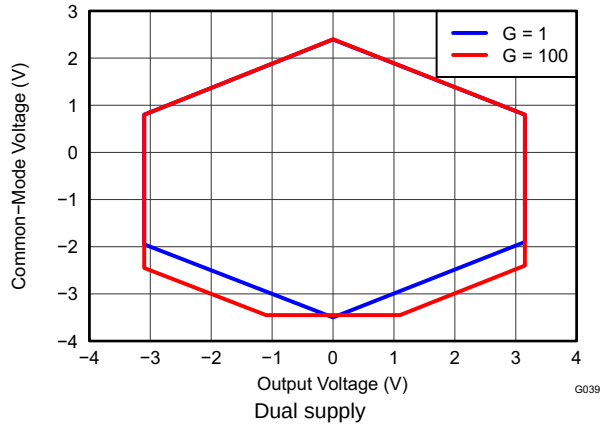


Figure 13. Input Common-Mode Voltage vs Output Voltage

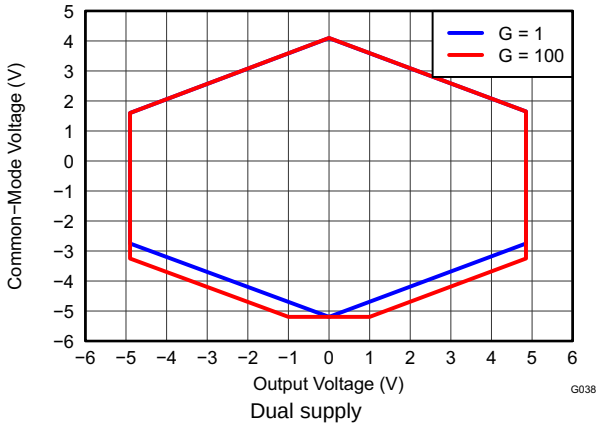


Figure 14. Input Common-Mode Voltage vs Output Voltage

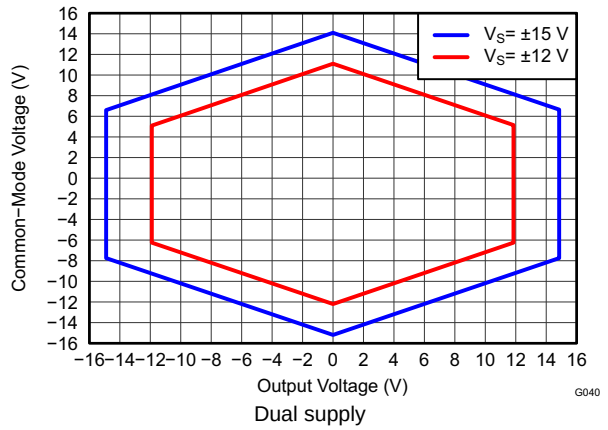


Figure 15. Input Common-Mode Voltage vs Output Voltage

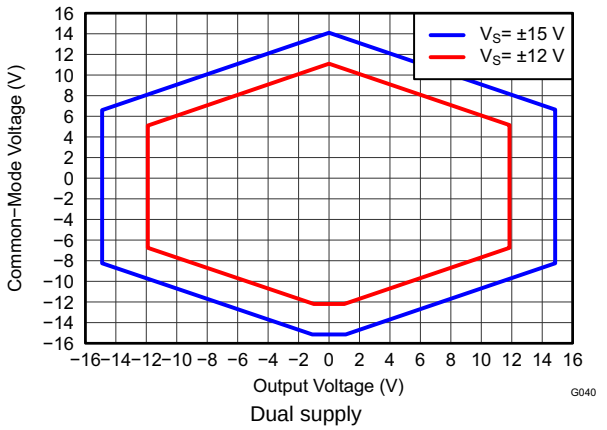


Figure 16. Input Common-Mode Voltage vs Output Voltage

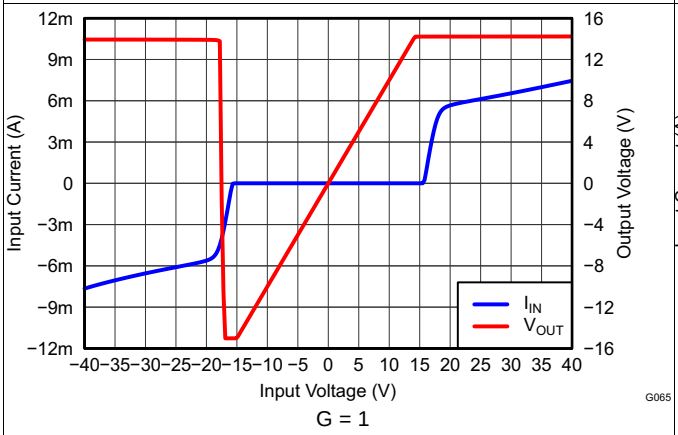


Figure 17. Input Overvoltage vs Input Current

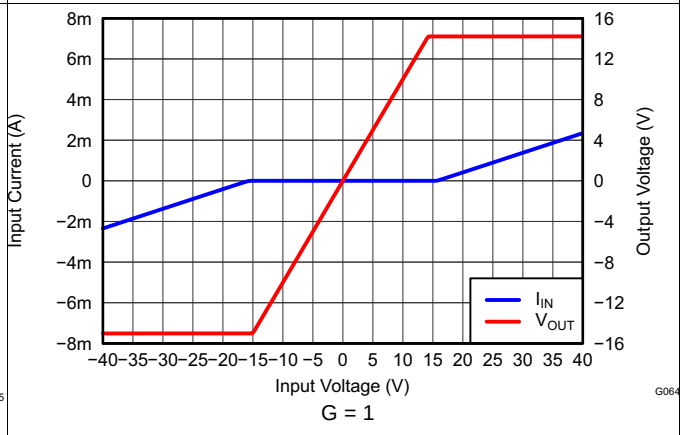


Figure 18. Input Overvoltage vs Input Current With 10-kΩ Resistance

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

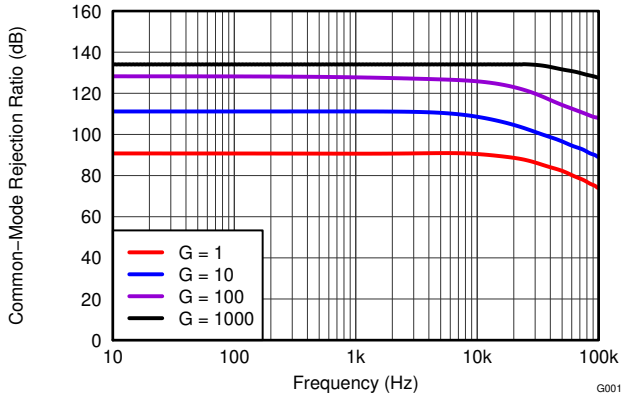


Figure 19. CMRR vs Frequency (RTI)

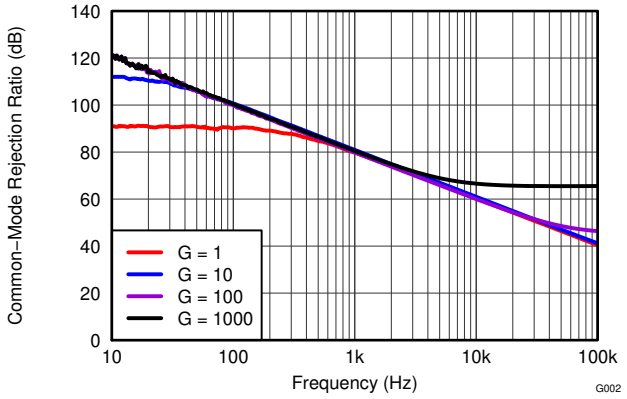


Figure 20. CMRR vs Frequency (RTI, 1-kΩ Source Imbalance)

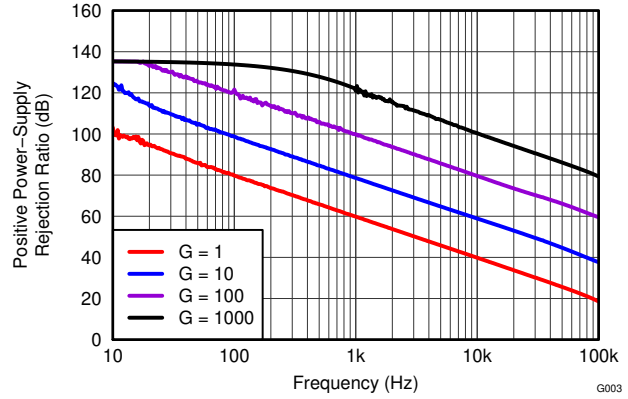


Figure 21. Positive PSRR vs Frequency (RTI)

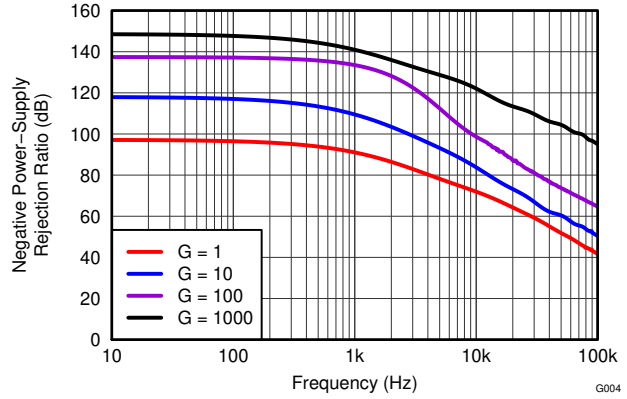


Figure 22. Negative PSRR vs Frequency (RTI)

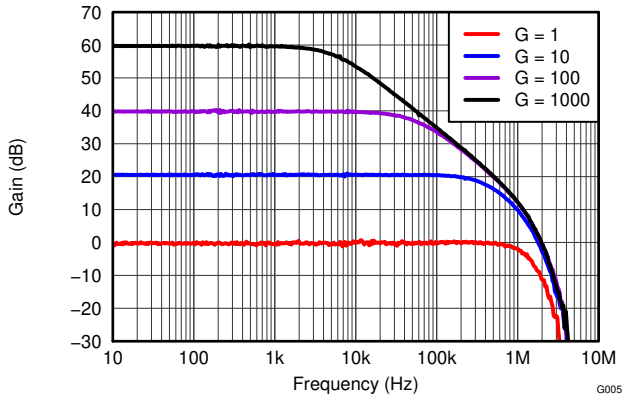


Figure 23. Gain vs Frequency

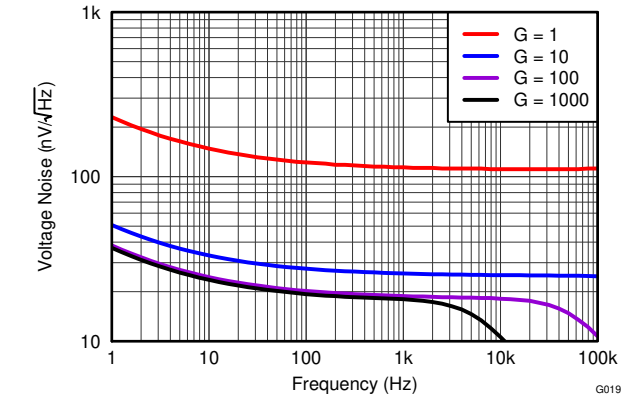


Figure 24. Voltage Noise Spectral Density vs Frequency (RTI)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

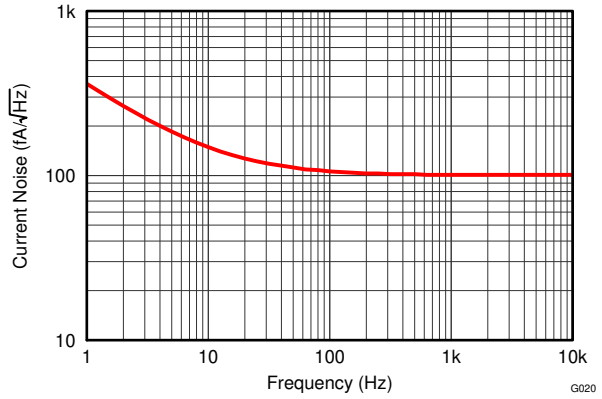


Figure 25. Current Noise Spectral Density vs Frequency (RTI)

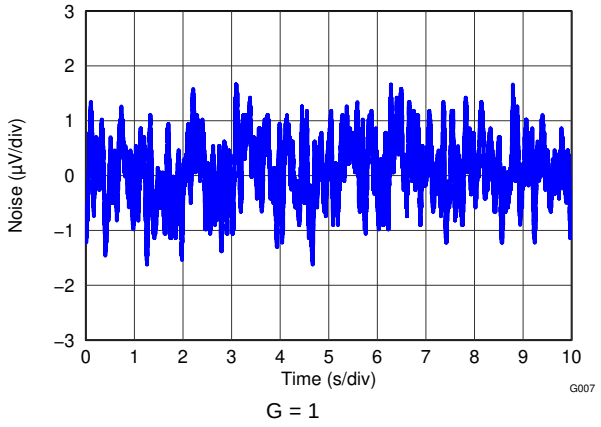


Figure 26. 0.1-Hz to 10-Hz RTI Voltage Noise

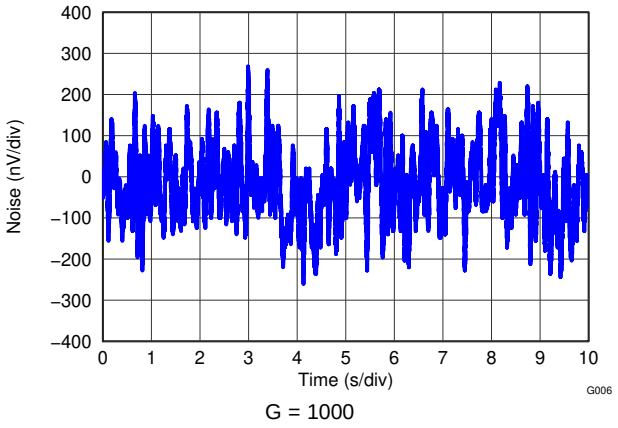


Figure 27. 0.1-Hz to 10-Hz RTI Voltage Noise

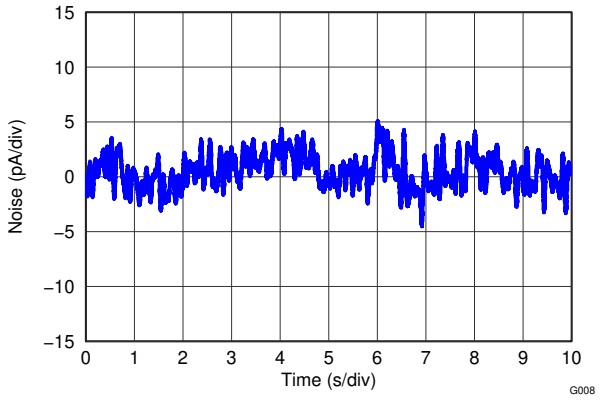


Figure 28. 0.1-Hz to 10-Hz RTI Current Noise

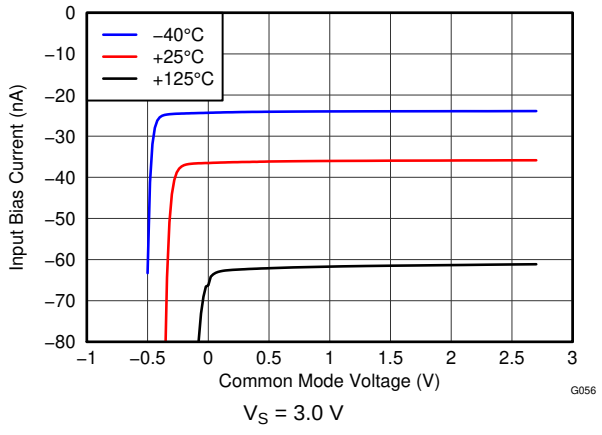


Figure 29. Input Bias Current vs Common-Mode Voltage

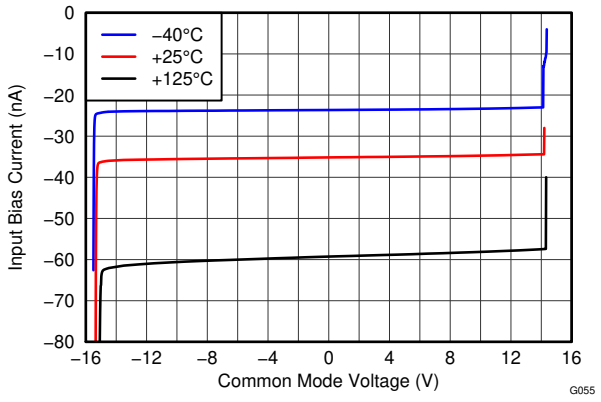


Figure 30. Input Bias Current vs Common-Mode Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

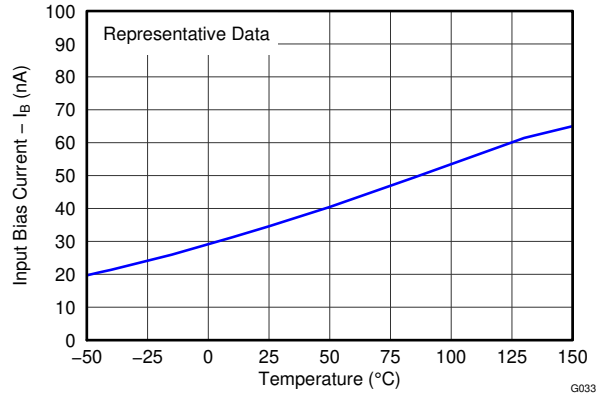


Figure 31. Input Bias Current vs Temperature

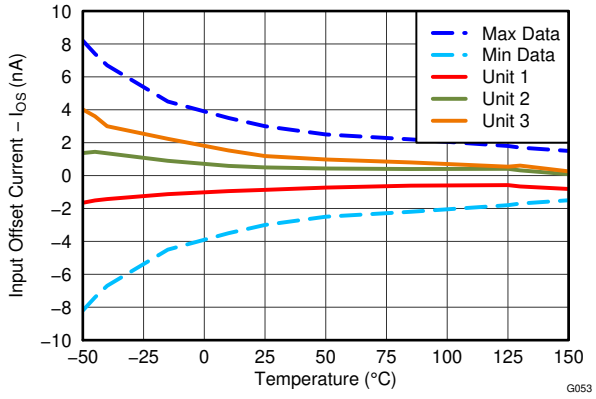


Figure 32. Input Offset Current vs Temperature

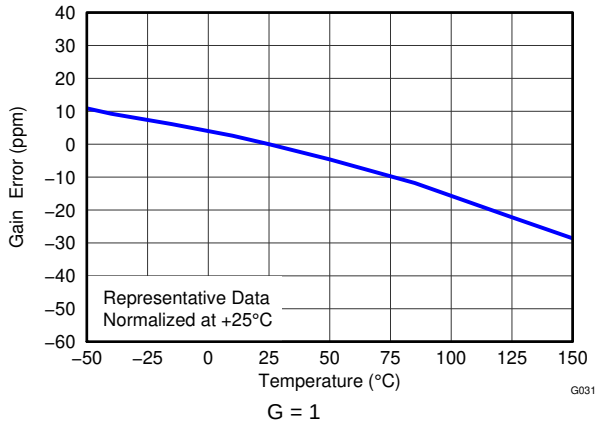


Figure 33. Gain Error vs Temperature

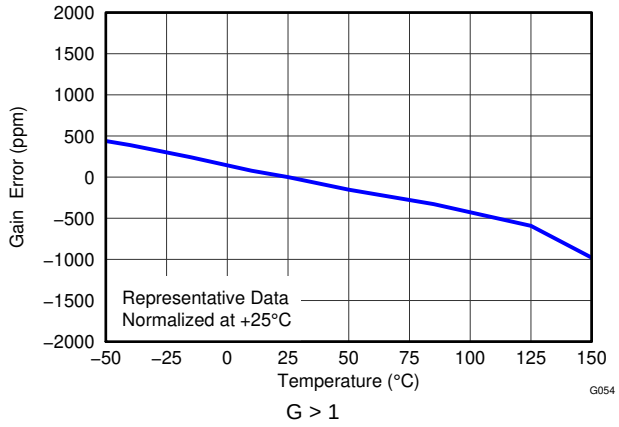


Figure 34. Gain Error vs Temperature

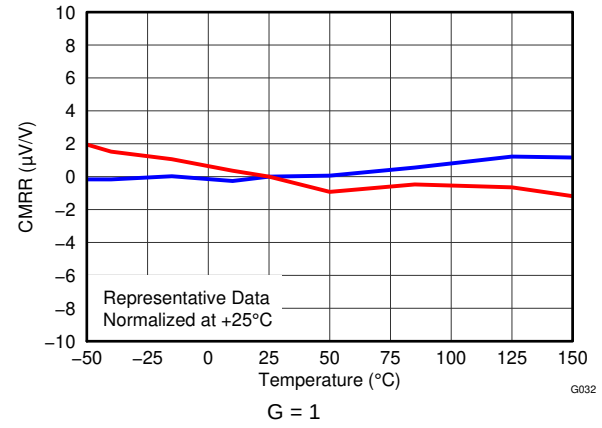


Figure 35. CMRR vs Temperature

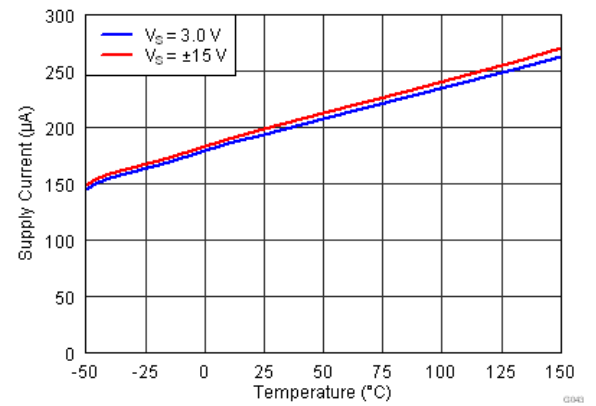


Figure 36. Supply Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

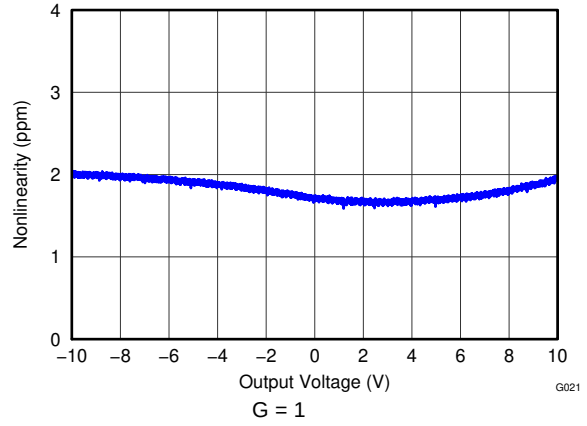


Figure 37. Gain Nonlinearity

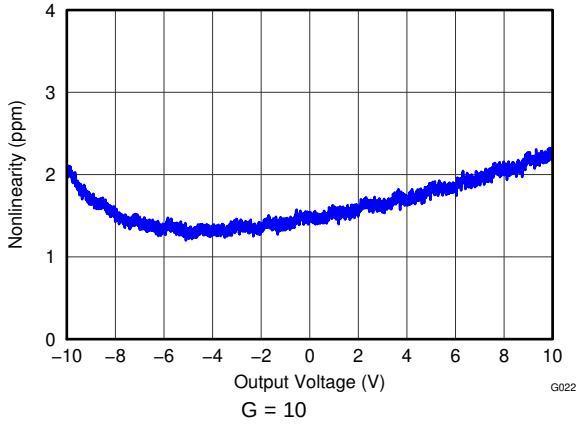


Figure 38. Gain Nonlinearity

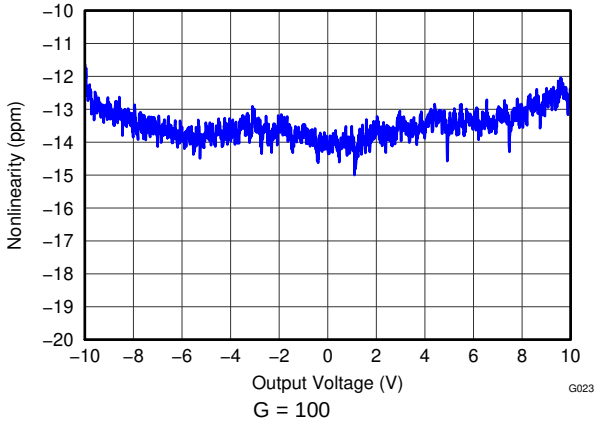


Figure 39. Gain Nonlinearity

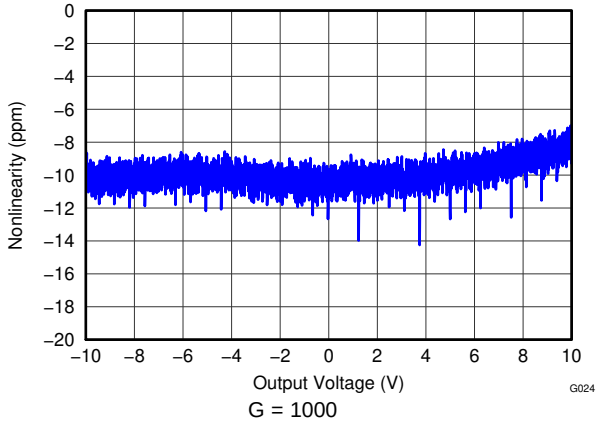


Figure 40. Gain Nonlinearity

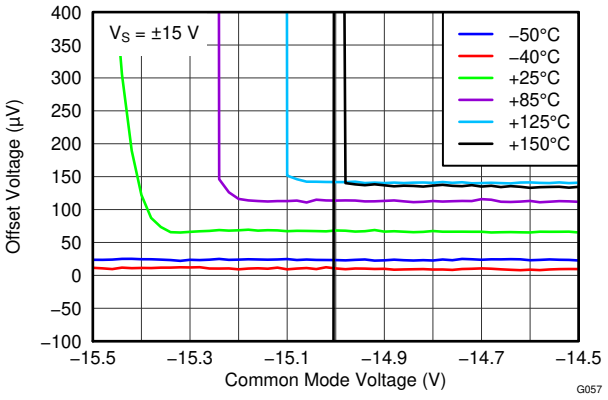


Figure 41. Offset Voltage vs Negative Common-Mode Voltage

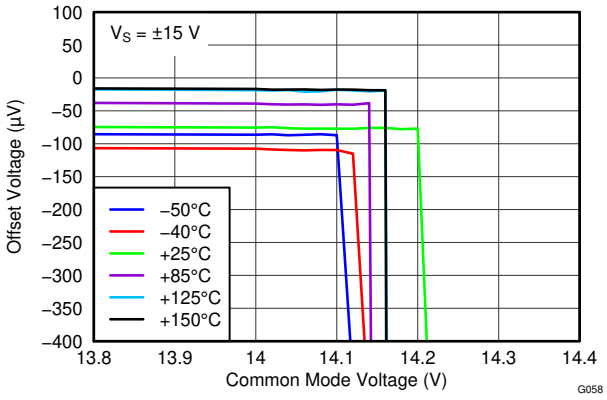


Figure 42. Offset Voltage vs Positive Common-Mode Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

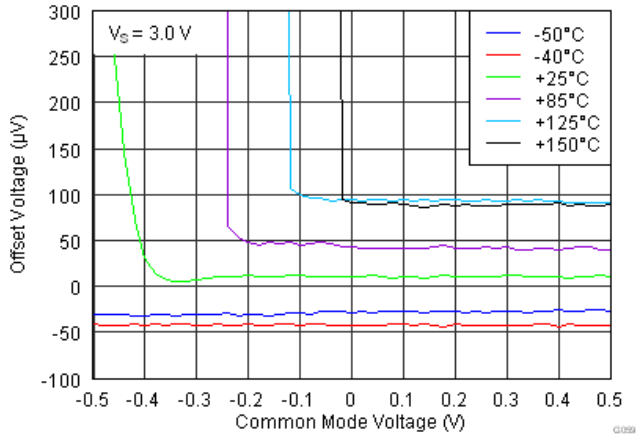


Figure 43. Offset Voltage vs Negative Common-Mode Voltage

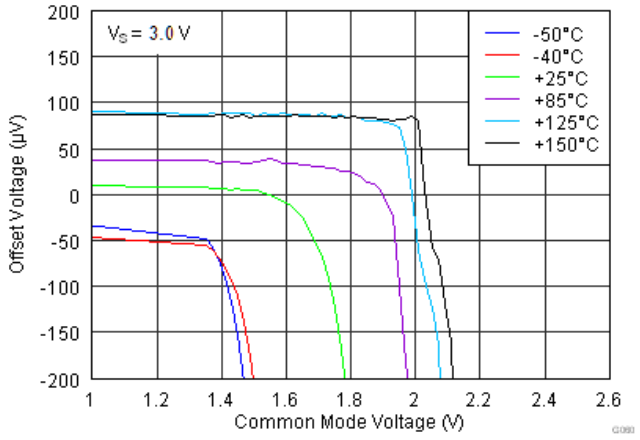


Figure 44. Offset Voltage vs Positive Common-Mode Voltage

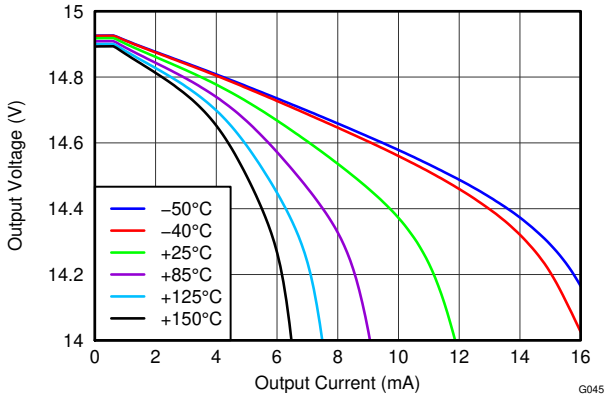


Figure 45. Positive Output Voltage Swing vs Output Current

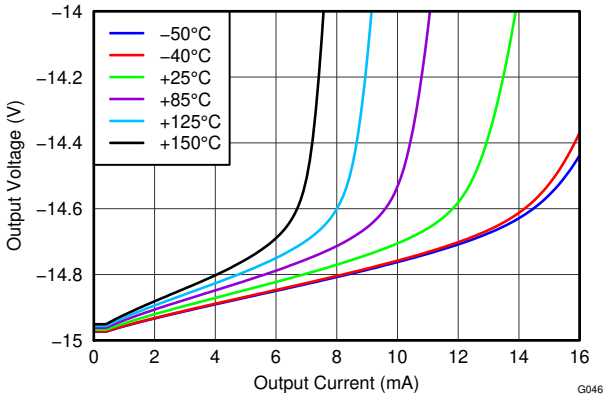


Figure 46. Negative Output Voltage Swing vs Output Current

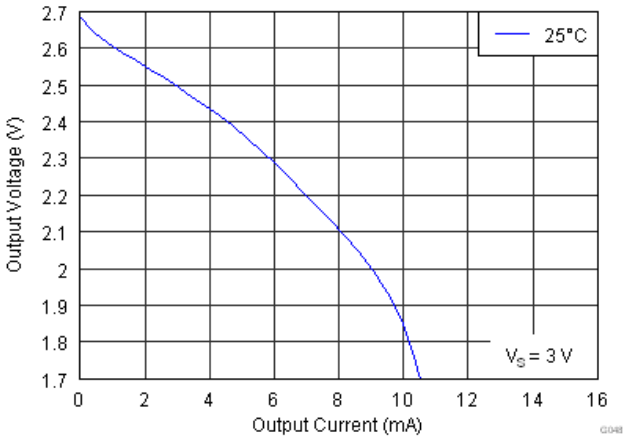


Figure 47. Positive Output Voltage Swing vs Output Current

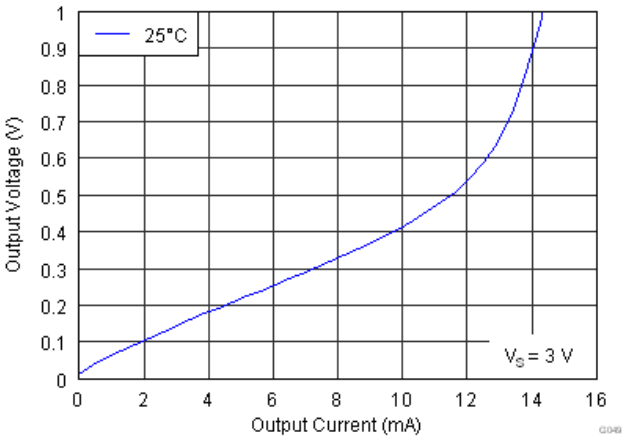


Figure 48. Negative Output Voltage Swing vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

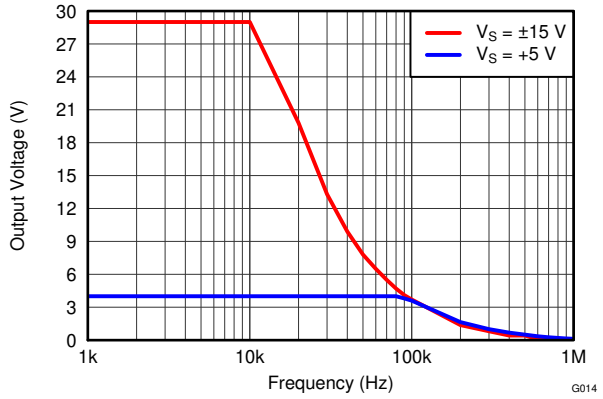


Figure 49. Large-Signal Frequency Response

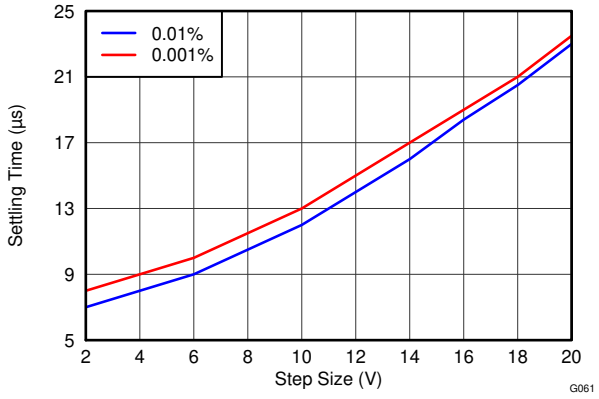
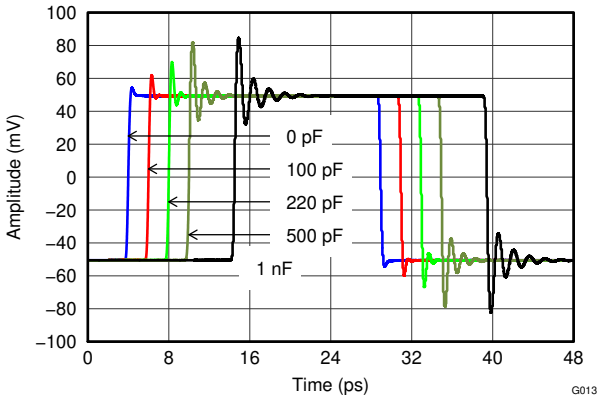
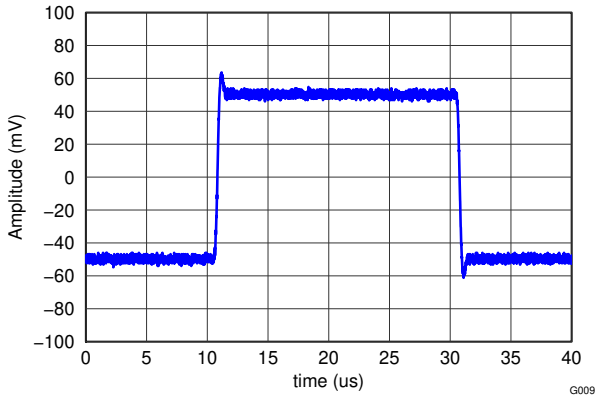


Figure 50. Settling Time vs Step Size



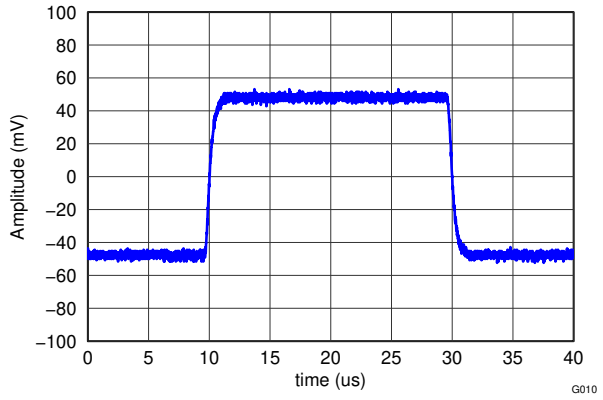
G = 1

Figure 51. Small-Signal Response Over Capacitive Loads



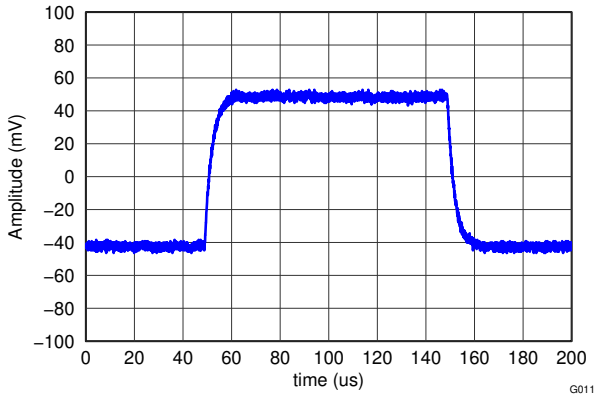
G = 1, R_L = 1 kΩ, C_L = 100 pF

Figure 52. Small-Signal Response



G = 10, R_L = 10 kΩ, C_L = 100 pF

Figure 53. Small-Signal Response



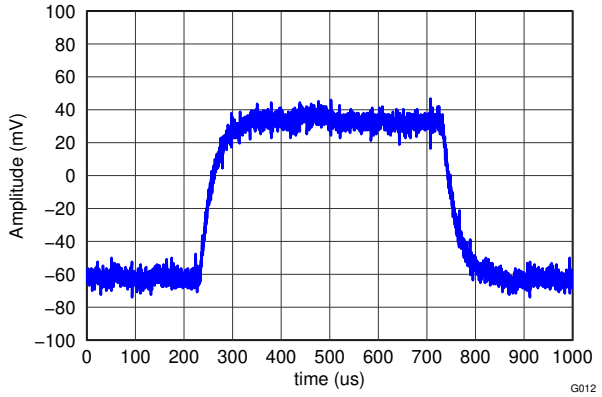
G = 100, R_L = 10 kΩ, C_L = 100 pF

Figure 54. Small-Signal Response

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 1000, R_L = 10 kΩ, C_L = 100 pF

Figure 55. Small-Signal Response

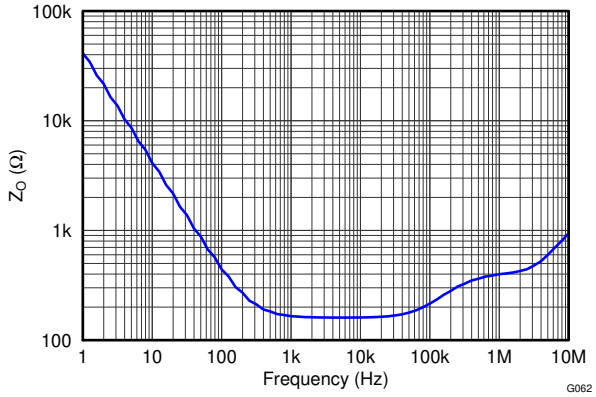


Figure 56. Open-Loop Output Impedance

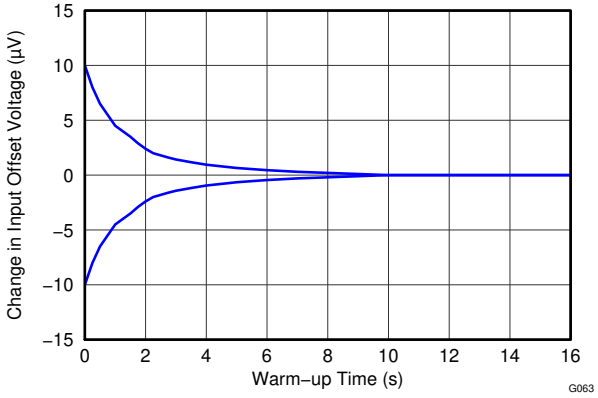


Figure 57. Change in Input Offset Voltage vs Warm-Up Time

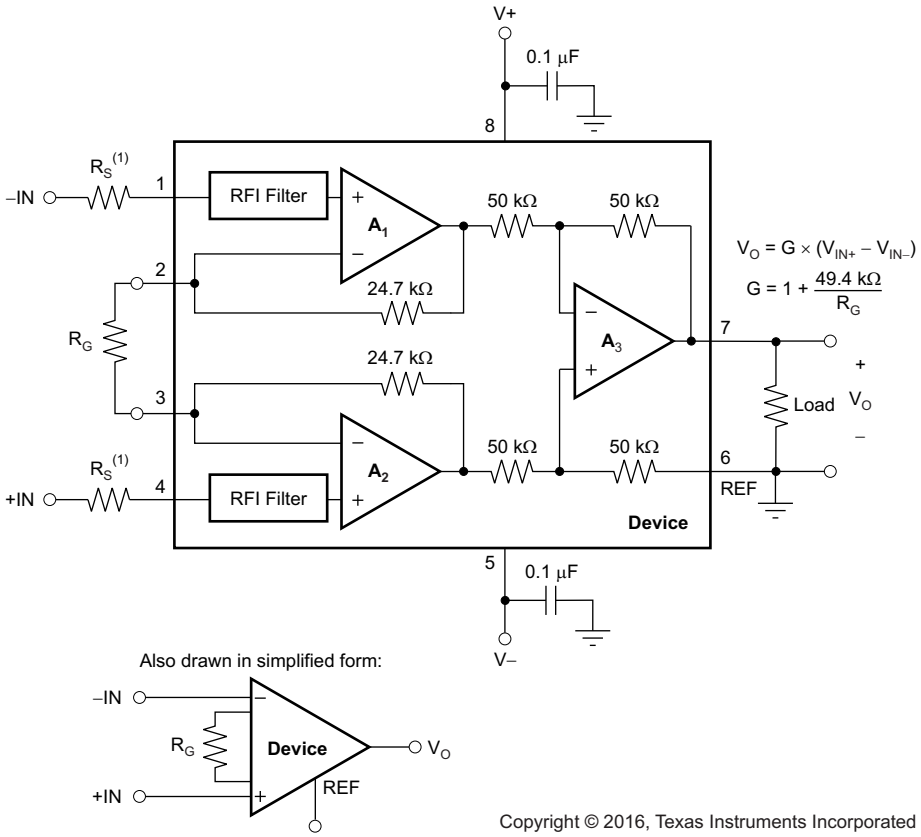
8 Detailed Description

8.1 Overview

The *Functional Block Diagram* section shows the basic connections required for operation of the INA826. Good layout practice mandates the use of bypass capacitors placed as close to the device pins as possible.

The output of the INA826 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. Although 5 Ω or less of stray resistance can be tolerated when maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

8.2 Functional Block Diagram



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(1) This resistor is optional if the input voltage stays above [(V–) – 2 V] or if the signal source current drive capability is limited to less than 3.5 mA; see the *Input Protection* section for more details.

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8.3 Feature Description

8.3.1 Inside the INA826

See the *Functional Block Diagram* section for a simplified representation of the INA826. A more detailed diagram, shown in Figure 58, provides additional insight into the INA826 operation.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

The differential input voltage is buffered by Q_1 and Q_2 and is impressed across R_G, causing a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF terminal.

The equations shown in Figure 58 describe the output voltages of A_1 and A_2. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V higher than the input voltages.

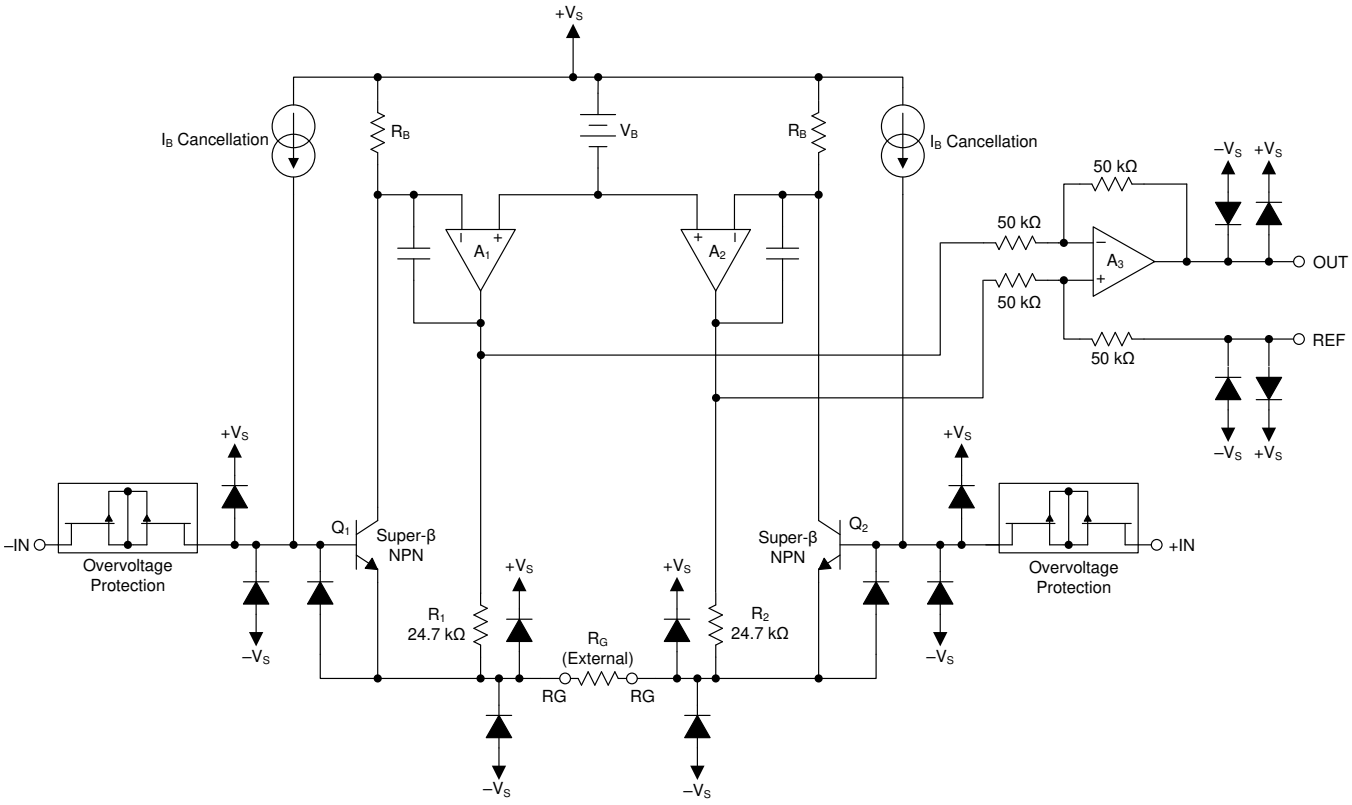


Figure 58. INA826 Simplified Circuit Diagram

Feature Description (continued)

8.3.2 Setting the Gain

Gain of the INA826 is set by a single external resistor, R_G, connected between pins 2 and 3. The value of R_G is selected according to Equation 1:

$$G = 1 + \left(\frac{49.4\ k\Omega}{R_G} \right) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 49.4-kΩ term in Equation 1 comes from the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA826.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
1	—	—
2	49.4 k	49.9 k
5	12.35 k	12.4 k
10	5.489 k	5.49 k
20	2.600 k	2.61 k
50	1.008 k	1 k
100	499	499
200	248	249
500	99	100
1000	49.5	49.9

8.3.2.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift is directly inferred from the gain of Equation 1.

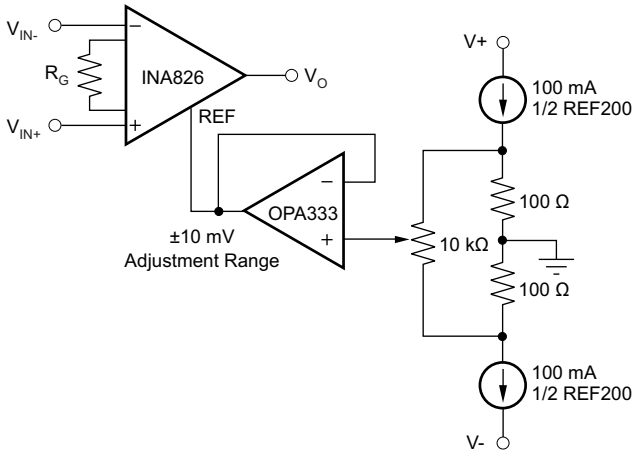
The best gain drift of 1 ppm/°C is achieved when the INA826 uses G = 1 without R_G connected. In this case, the gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 50-kΩ resistors in the differential amplifier (A_3). At G greater than 1, the gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. Process improvements of the temperature coefficient of the feedback resistors now make possible specifying a maximum gain drift of the feedback resistors of 35 ppm/°C, thus significantly improving the overall temperature stability of applications using gains greater than 1.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see Figure 19 and Figure 20.

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8.3.3 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 59 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.



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Figure 59. Optional Trimming of the Output Offset Voltage

8.3.4 Input Common-Mode Range

The linear input voltage range of the INA826 input circuitry extends from the negative supply voltage to 1 V below the positive supply and maintains 84-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is described in the input common-mode voltage versus output voltage *Typical Characteristics* curves (Figure 9 through Figure 15) and the offset voltage versus common-mode voltage curves (Figure 41 through Figure 43). The INA826 operates over a wide range of power supplies and V_{REF} configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2, which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see Figure 58) provides a check for the most common overload conditions. The designs of A_1 and A_2 are identical and the outputs can swing to within approximately 100 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 can still be in linear operation, responding to changes in the noninverting input voltage. This difference can give the appearance of linear operation but the output voltage is invalid.

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA826 employs a current-feedback topology with PNP input transistors; see Figure 58. The matched PNP transistors Q_1 and Q_2 shift the input voltages of both inputs up by a diode drop, and (through the feedback network) shift the output of A_1 and A_2 by approximately 0.8 V. With both inputs and V_{REF} at single-supply ground (negative power supply), the output of A_1 and A_2 is well within the linear range, allowing differential measurements to be made at the GND level. As a result of this input level-shifting, the voltages at pin 2 and pin 3 are not equal to the respective input terminal voltages (pin 1 and pin 4). For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

8.3.5 Input Protection

The inputs of the INA826 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. However, if the input voltage exceeds (V–) – 2 V and the signal source current drive capability exceeds 3.5 mA, the output voltage switches to the opposite polarity; see Figure 17. This polarity reversal can easily be avoided by adding resistance of 10 kΩ in series with both inputs.

Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 8 mA. Figure 17 and Figure 18 illustrate this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

8.3.6 Input Bias Current Return Path

The input impedance of the INA826 is extremely high (approximately 20 GΩ). However, a path must be provided for the input bias current of both inputs. This input bias current is typically 35 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 60 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA826 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in Figure 60). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

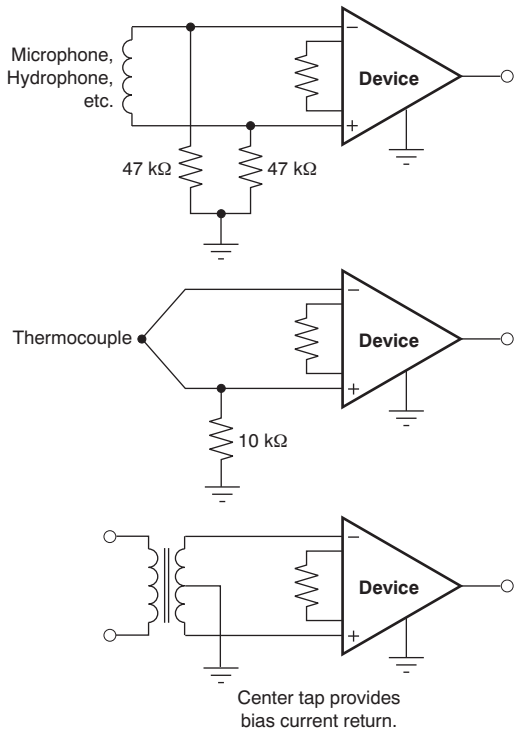


Figure 60. Providing an Input Common-Mode Current Path

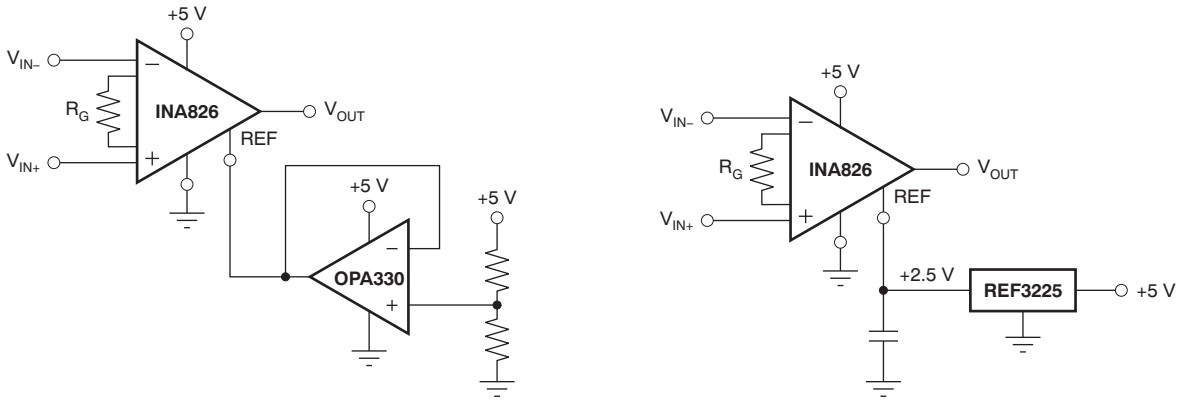
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8.3.7 Reference Terminal

The output voltage of the INA826 is developed with respect to the voltage on the reference pin. Often in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level can be useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, tie a voltage source to the REF pin to level-shift the output so that the INA826 can drive a single-supply ADC, for example.

For best performance, keep the source impedance to the REF pin less than 5 Ω. As illustrated in the *Functional Block Diagram* section, the reference resistor is at one end of a 50-kΩ resistor. Additional impedance at the REF pin adds to this 50-kΩ resistor. The imbalance in the resistor ratios results in degraded common-mode rejection ratio (CMRR).

Figure 61 shows two different methods of driving the reference pin with low impedance. The OPA330 is a low-power, chopper-stabilized amplifier, and therefore offers excellent stability over temperature. The OPA330 is available in the space-saving SC70 and even smaller chip-scale package. The REF3225 is a precision reference in the small SOT23-6 package.



a) Level shifting using the OPA330 as a low-impedance buffer

b) Level shifting using the low-impedance output of the REF3225

Figure 61. Options for Low-Impedance Level Shifting

8.3.8 Dynamic Performance

Figure 23 illustrates that, despite its low quiescent current of only 200 µA, the INA826 achieves much wider bandwidth than other INAs in its class. This achievement is a result of using TI's proprietary high-speed precision bipolar process technology. The current-feedback topology provides the INA826 with wide bandwidth even at high gains. Settling time also remains excellent at high gain because of a high slew rate of 1 V/µs.

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8.3.9 Operating Voltage

The INA826 operates over a power-supply range of 3 V to 36 V (±1.5 V to ±18 V). Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.3.9.1 Low-Voltage Operation

The INA826 can operate on power supplies as low as ±1.5 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very-low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Figure 9 through Figure 15 and Figure 41 through Figure 43 describe the range of linear operation for various supply voltages, reference connections, and gains.

8.3.10 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimizing these errors is important. Make sure to choose high-precision components, such as the INA826, that have improved specifications in critical areas that impact the precision of the overall system. Figure 62 shows an example application.

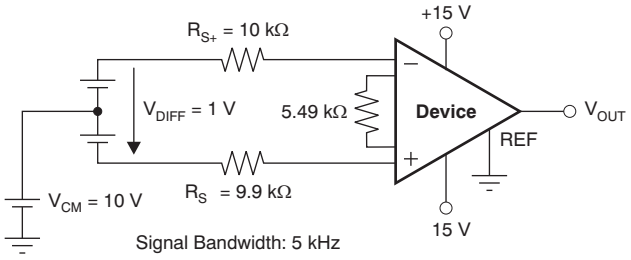


Figure 62. Example Application With G = 10 V/V and 1-V Differential Voltage

Resistor-adjustable INAs, such as the INA826, show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

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The INA826 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). Table 2 summarizes the major error sources in common INA applications and compares the two cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor). As can be seen in Table 2, although the static errors (absolute accuracy errors) in G = 1 are almost twice as great as compared to G = 10, there are much fewer drift errors because of the much lower gain error drift. In most applications, these static errors can readily be removed during calibration in production. All calculations refer the error to the input for easy comparison and system evaluation.

Table 2. Error Calculations

ERROR SOURCE	ERROR CALCULATION	INA826		
		SPECIFICATION	G = 10 ERROR (ppm)	G = 1 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C				
Input offset voltage (µV)	V_{OSI} / V_{DIFF}	150	150	150
Output offset voltage (µV)	V_{OSO} / (G × V_{DIFF})	700	70	700
Input offset current (nA)	I_{OS} × maximum (R_{S+}, $R_{S–}$) / V_{DIFF}	5	50	50
CMRR (dB)	V_{CM} / ($10^{CMRR/20}$ × V_{DIFF})	104 (G = 10), 84 (G = 1)	63	631
Total absolute accuracy error (ppm)			333	1531
DRIFT TO 105°C				
Gain drift (ppm/°C)	GTC × (T_A – 25)	35 (G = 10), 1 (G = 1)	2800	80
Input offset voltage drift (µV/°C)	(V_{OSI_TC} / V_{DIFF}) × (T_A – 25)	2	160	160
Output offset voltage drift (µV/°C)	[V_{OSO_TC} / (G × V_{DIFF})] × (T_A – 25)	10	80	800
Offset current drift (pA/°C)	I_{OS_TC} × maximum (R_{S+}, $R_{S–}$) × (T_A – 25) / V_{DIFF}	60	48	48
Total drift error (ppm)			3088	1088
RESOLUTION				
Gain nonlinearity (ppm of FS)		5	5	5
Voltage noise (1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2 \times \frac{6}{V_{DIFF}}}$	e_{NI} = 18, e_{NO} = 110	10	10
Total resolution error (ppm)			15	15
TOTAL ERROR				
Total error	Total error = sum of all error sources		3436	2634

8.4 Device Functional Modes

The INA826 has a single functional mode and is operational when the power-supply voltage is greater than 3 V (±1.5 V). The maximum power-supply voltage for the INA826 is 36 V (±18 V).

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The low power consumption and high performance of the INA826 make the device an excellent instrumentation amplifier for many applications. The INA826 can be used in many low-power, portable applications because the device has a low quiescent current (200 µA, typical) and comes in a small 8-pin WSON package. The input protection circuitry, low maximum gain drift, low offset voltage, and 36-V maximum supply voltage also make the INA826 an excellent choice for industrial applications as well.

9.2 Typical Application

Figure 63 shows a three-terminal programmable-logic controller (PLC) design for the INA826. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

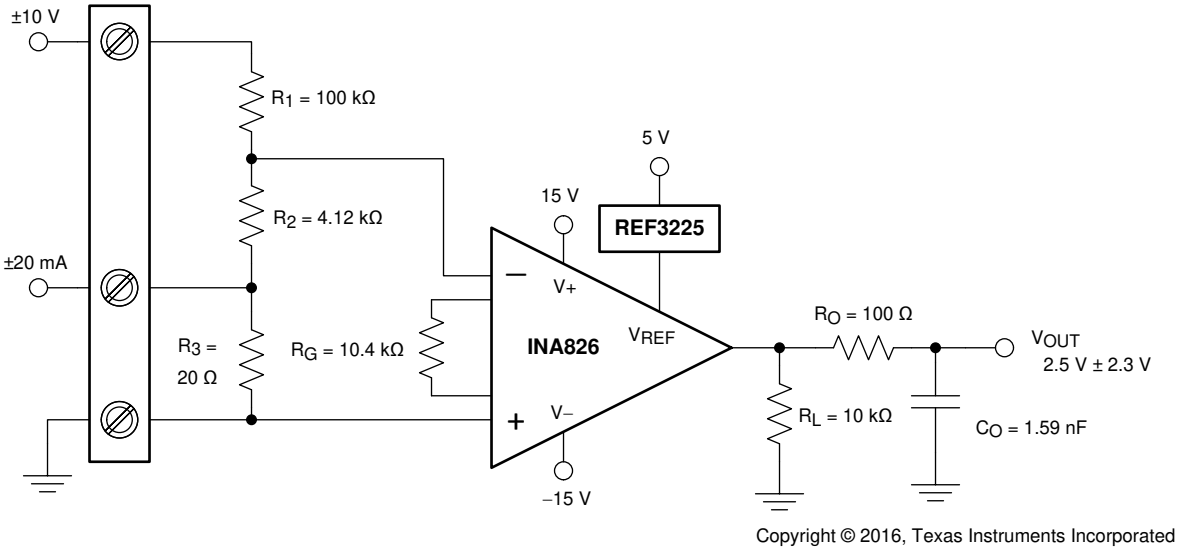


Figure 63. Three-Terminal PLC Design

9.2.1 Design Requirements

This design has the following requirements:

- Supply voltage: ±15 V, 5 V
- Inputs: ±10 V, ±20 mA
- Output: 2.5 V, ±2.3 V

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Typical Application (continued)

9.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 63: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, the current input mode transfer function is given by Equation 2.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (2)$$

where

- G represents the gain of the instrumentation amplifier

The transfer function for the voltage input mode is shown by Equation 3.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (3)$$

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. This value is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Equation 4 can be used to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \quad (4)$$

The value obtained from Equation 4 is not a standard 0.1% value, so 4.12 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

The ideal gain of the instrumentation amplifier is calculated with Equation 5.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \quad (5)$$

Using the INA826 gain equation, Equation 1, the gain-setting resistor value is calculated as shown by Equation 6.

$$G_{INA826} = 1 + \frac{49.4\ k\Omega}{R_G} \rightarrow R_G = \frac{49.4\ k\Omega}{G_{INA826} - 1} = \frac{49.4\ k\Omega}{5.75 - 1} = 10.4\ k\Omega \quad (6)$$

10.4 kΩ is a standard 0.1% resistor value that can be used in this design. Finally, the output RC filter components are selected to have a –3-dB cutoff frequency of 1 MHz.

9.2.3 Application Curves

Figure 64 and Figure 65 illustrate typical characteristic curves for Figure 63.

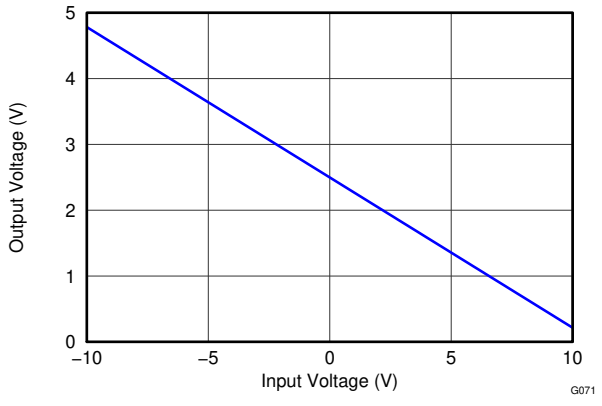


Figure 64. PLC Output Voltage vs Input Voltage

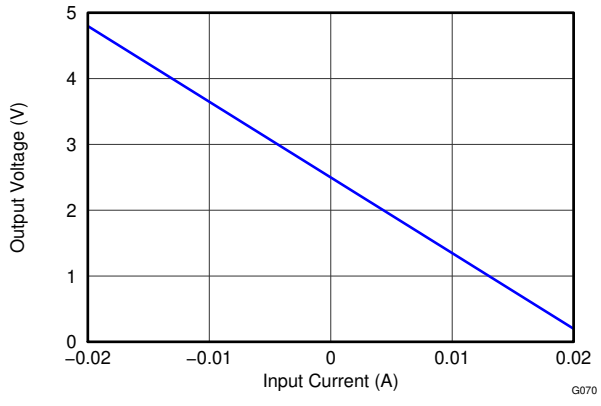


Figure 65. PLC Output Voltage vs Input Current

9.3 System Examples

9.3.1 Circuit Breaker

Figure 66 shows the INA826 used in a circuit breaker application.

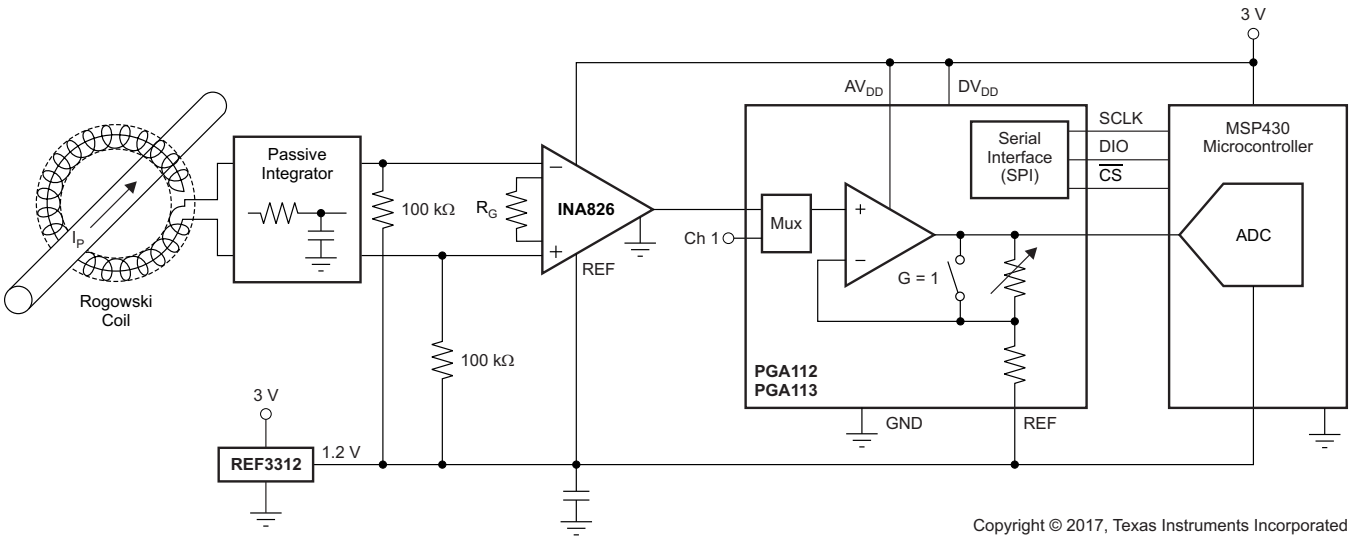


Figure 66. Circuit Breaker Example

9.3.2 Programmable Logic Controller (PLC) Input

The INA826 used in an example programmable logic controller (PLC) input application is shown in Figure 67.

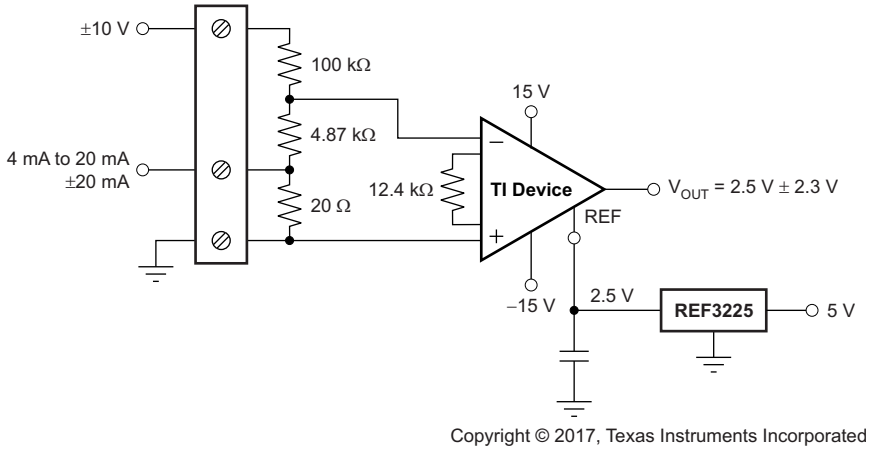


Figure 67. ±10-V, 4-mA to 20-mA PLC Input

Additional application ideas are illustrated in Figure 68 to Figure 72.

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System Examples (continued)

9.3.3 Using TINA-TI SPICE-Based Analog Simulation Program With the INA826

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

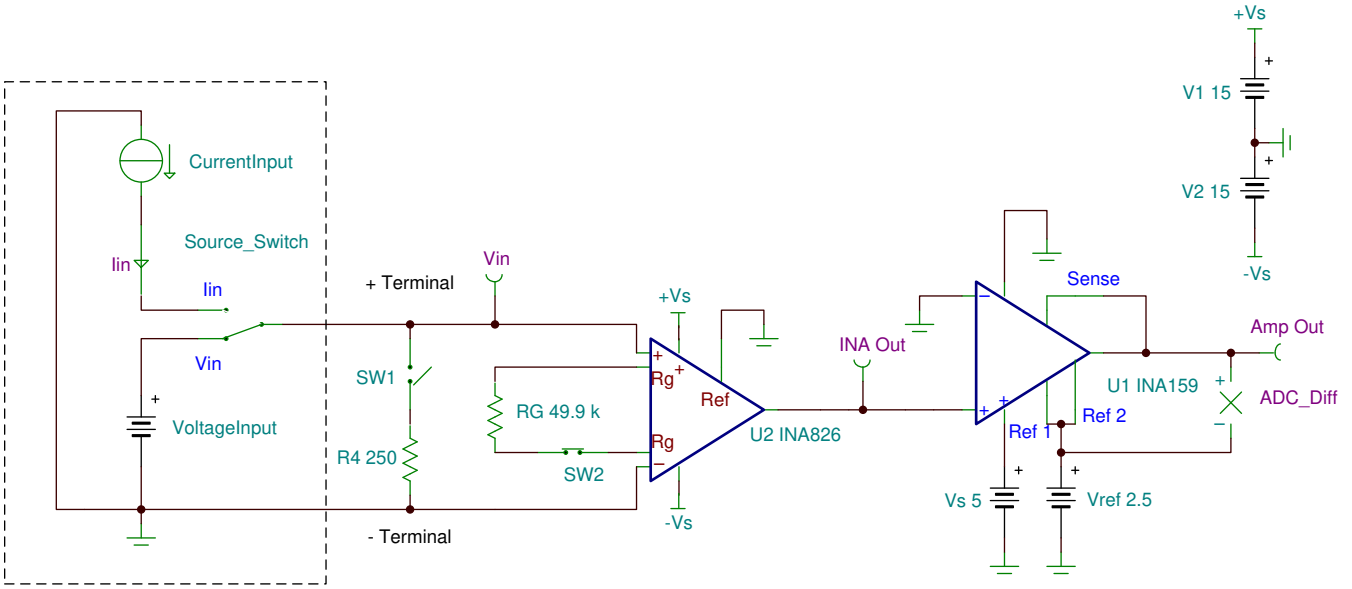
Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 68 and Figure 70 illustrate example TINA-TI circuits for the INA826 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are provided in this section.

NOTE

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

The circuit in Figure 68 is used to convert inputs of ±10 V, ±5 V, or ±20 mA to an output voltage range from 0.5 V to 4.5 V. The input selection depends on the settings of SW_1 and SW_2. Further explanation as well as the TINA-TI simulation circuit is provided in the compressed file that can be downloaded at the following link: *PLC Circuit*.



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Figure 68. Two-Terminal Programmable Logic Controller (PLC) Input

Figure 69 is an example of a LEAD I ECG circuit. The input signals come from leads attached to the right arm (RA) and left arm (LA). These signals are simulated with the circuitry in the corresponding boxes. Protection resistors (R_{PROT1} and R_{PROT2}) and filtering are also provided. The OPA333 is used as an integrator to remove the gained-up dc offsets and servo the INA826 outputs to V_{REF}. Finally, the right leg drive is biased to a potential ($+V_S$ / 2), and inverts and amplifies the average common-mode signal back into the patient's right leg. This architecture reduces the 50-Hz and 60-Hz noise pickup.

System Examples (continued)

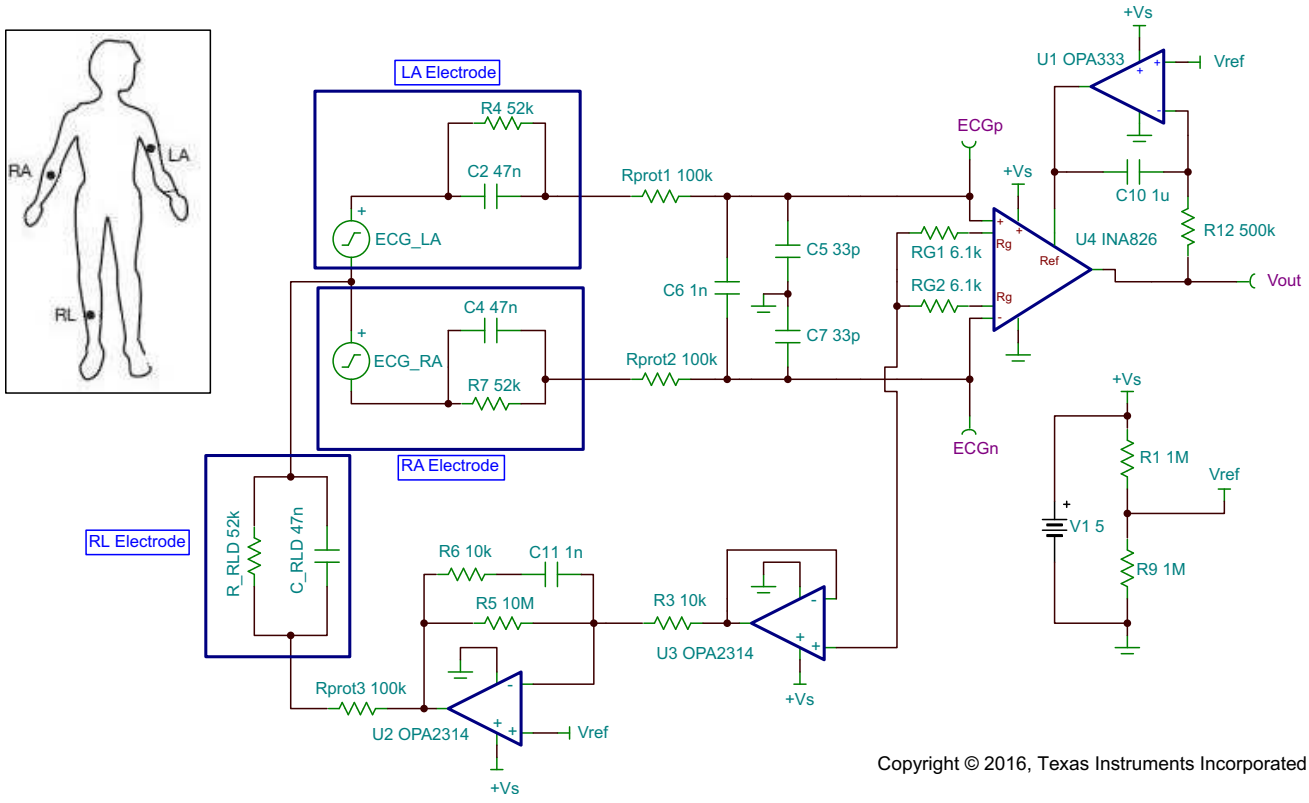


Figure 69. ECG Circuit

Figure 70 shows an example of how the INA826 can be used for low-side current sensing. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the INA826 with gain set to 100. The output swing of the INA826 is set by the common-mode voltage (which is 0 V in low-side current sensing) and power supplies. Therefore, a dual-supply circuit is implemented. The load current is set from 1 A to 10 A, corresponding to an output voltage range from 350 mV to 3.5 V. The output range can be adjusted by changing the shunt resistor and the gain of the INA826. Click the following link to download the TINA-TI file: *Current Sensing Circuit*.

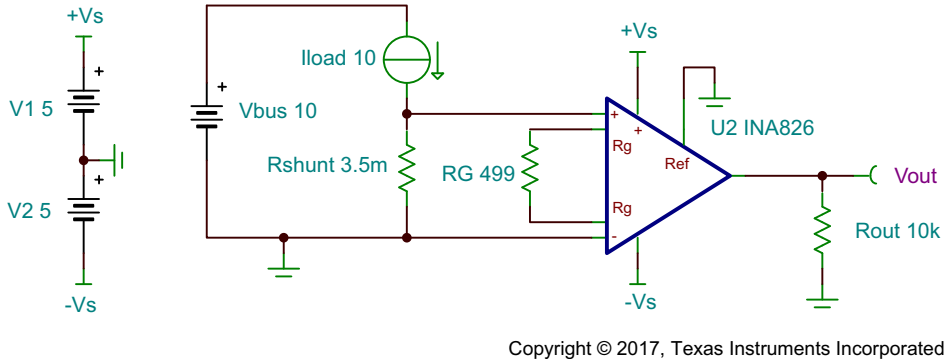


Figure 70. Low-Side Current Sensing

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System Examples (continued)

Figure 71 shows an example of how the INA826 can be used for RTD signal conditioning. This circuit creates an excitation current (I_{SET}) by forcing 2.5 V from the REF5025 across R_{SET}. The zero-drift, low-noise OPA188 creates the virtual ground that maintains a constant differential voltage across R_{SET} with changing common-mode voltage. This voltage is necessary because the voltage on the positive input of the INA826 fluctuates over temperature as a result of the changing RTD resistance. Click the following link to download the TINA-TI file: *RTD Circuit*.

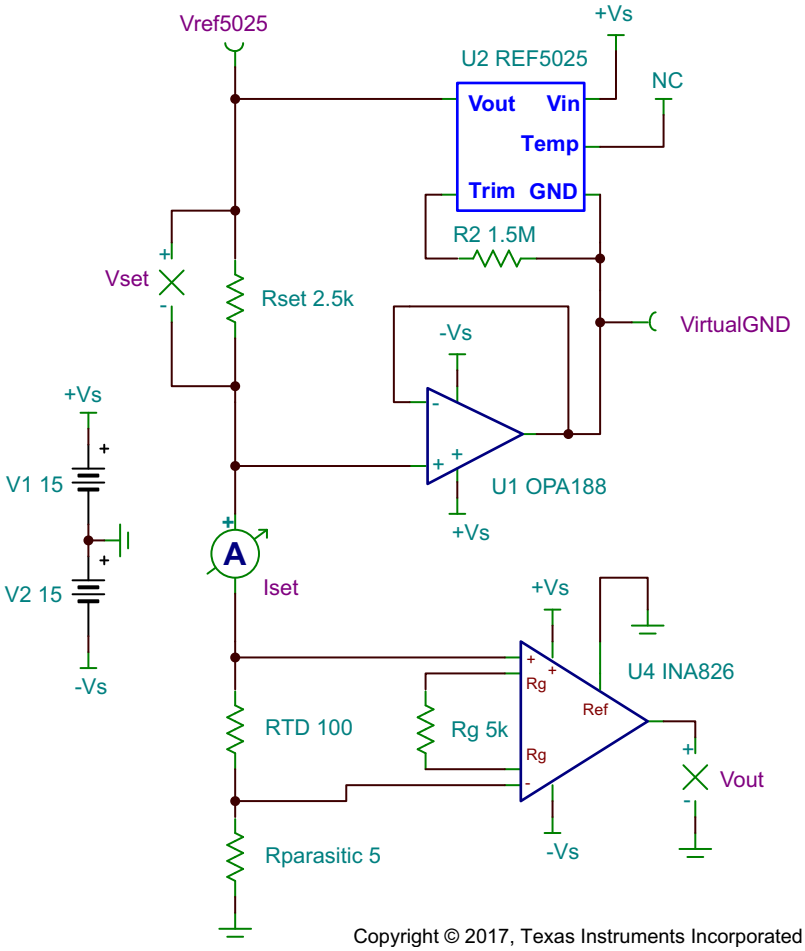
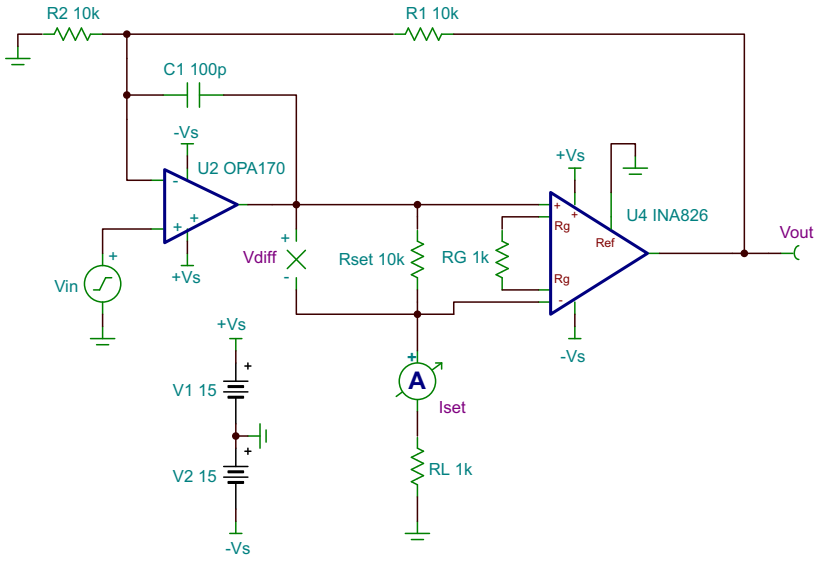


Figure 71. RTD Signal Conditioning

The circuit in Figure 72 creates a precision current I_{SET} by forcing the INA826 V_{DIFF} across R_{SET}. The input voltage V_{IN} is amplified to the output of the INA826 and then divided down by the gain of the INA826 to create V_{DIFF}. I_{SET} can be controlled either by changing the value of the gain-set resistor R_G, the set resistor R_{SET}, or by changing V_{OUT} through the gain of the composite loop. Make sure that the changing load resistance R_L does not create a voltage on the negative input of the INA826 that violates the compliance of the common-mode input range. Likewise, the voltage on the output of the OPA170 must remain compliant throughout the changing load resistance for this circuit to function properly.

System Examples (continued)



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Figure 72. Precision Current Source

10 Power Supply Recommendations

The nominal performance of the INA826 is specified with a supply voltage of ±15 V and mid-supply reference voltage. The device can also be operated using power supplies from ±1.5 V (3 V) to ±18 V (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the *Typical Characteristics* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place 0.1-μF bypass capacitors close to the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

The INA826EVM is intended to provide basic functional evaluation of the INA826. An image of the INA826EVM is provided in Figure 73. The INA826EVM is also available for purchase through the TI eStore.

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

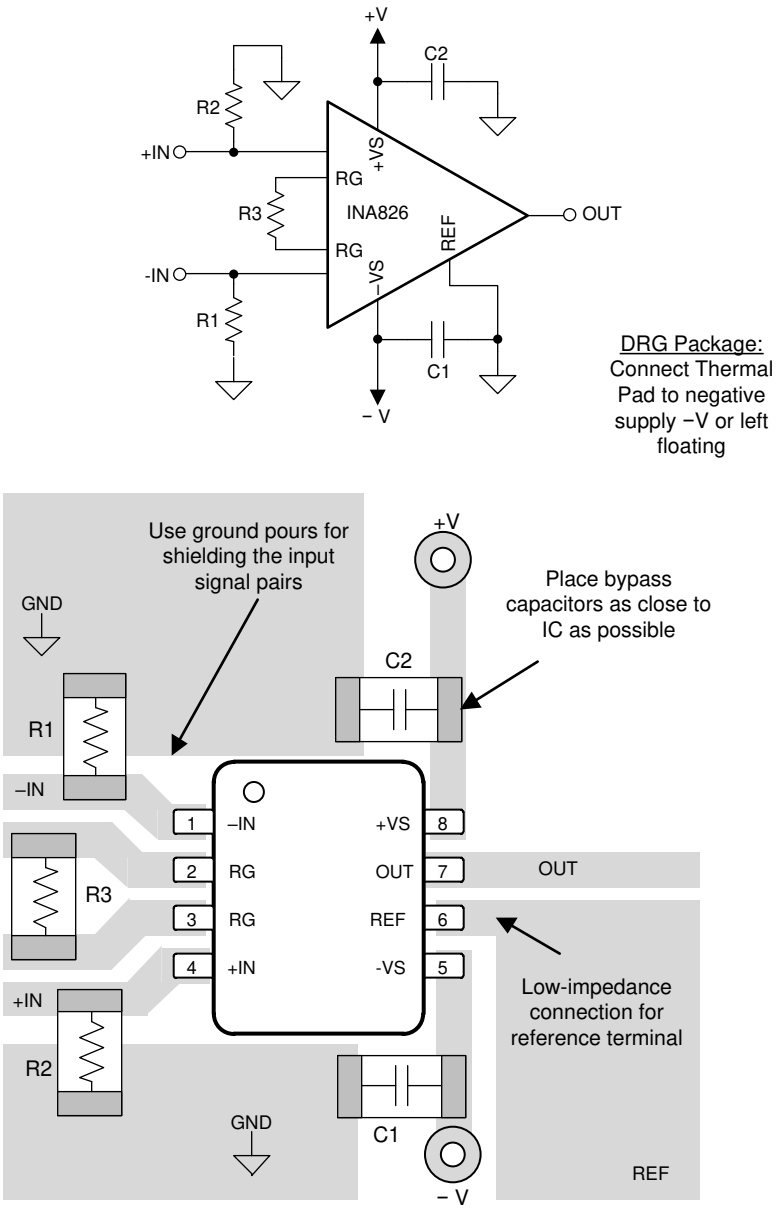
- Make sure to match both input paths to avoid converting common-mode signals into differential signals.
- Connect a bypass capacitor of 0.1-μF between each supply pin and ground, placed close to the device as possible.
- Route the input traces as far away from the supply or output traces as possible. This reduces parasitic coupling.
- Place the external components as close to the device as possible.
- Keep traces as short as possible.
- For the DRG package: Connect the exposed thermal pad to the lowest voltage potential on the circuit that is the negative power supply (–V).

11.1.1 CMRR vs Frequency

The INA826 pinout is optimized for achieving maximum CMRR performance over a wide range of frequencies. However, make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, choose the component so that the switch capacitance is as small as possible.

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11.2 Layout Example



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Figure 73. INA826 Example Layout

The INA826EVM provides the following features:

- Intuitive evaluation with silkscreen schematic
- Easy access to nodes with surface-mount test points
- Advanced evaluation with two prototype areas
- Reference voltage source flexibility
- Convenient input and output filtering

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPAx330 50-μV VOS, 0.25-μV/°C, 35-μA CMOS Operational Amplifiers Zerø-Drift Series* data sheet
- Texas Instruments, *REF32xx 4ppm/°C, 100μA, SOT23-6 Series Voltage Reference* data sheet
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *INA333 Micro-Power (50μA), Zerø-Drift, Rail-to-Rail Out Instrumentation Amplifier* data sheet
- Texas Instruments, *PGA280 Zerø-Drift, High-Voltage, Programmable Gain Instrumentation Amplifier* data sheet
- Texas Instruments, *INA159 Precision, Gain of 0.2 Level Translation Difference Amplifier* data sheet
- Texas Instruments, *PGA11x Zerø-Drift Programmable Gain Amplifier With Mux* data sheet
- Texas Instruments, *INA826EVM User's Guide*
- Texas Instruments, TINA-TI software folder

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA826AID	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AID.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AIDGK	Last Time Buy	Production	VSSOP (DGK) | 8	80 | BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDGK.B	Last Time Buy	Production	VSSOP (DGK) | 8	80 | BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI
INA826AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826
INA826AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IPEI
INA826AIDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IPEI
INA826AIDRGRG4	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IPEI
INA826AIDRGRG4.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IPEI
INA826AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI
INA826AIDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

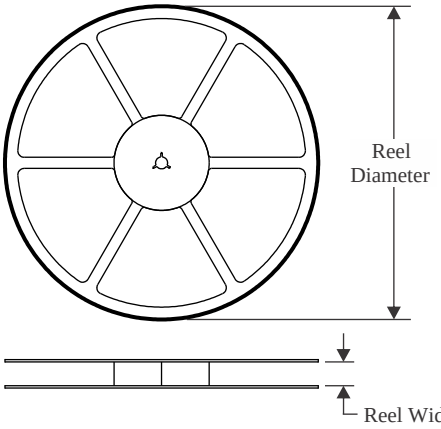
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

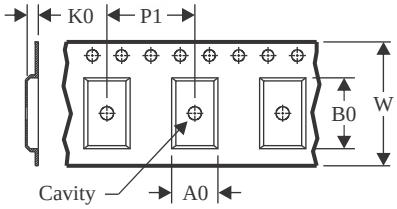
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

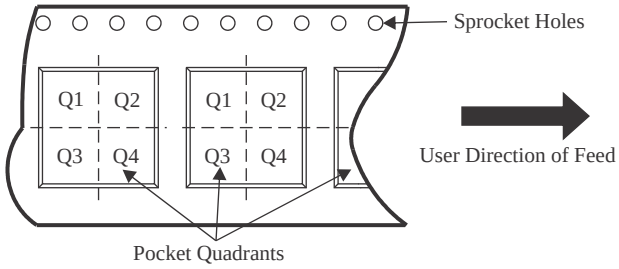


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

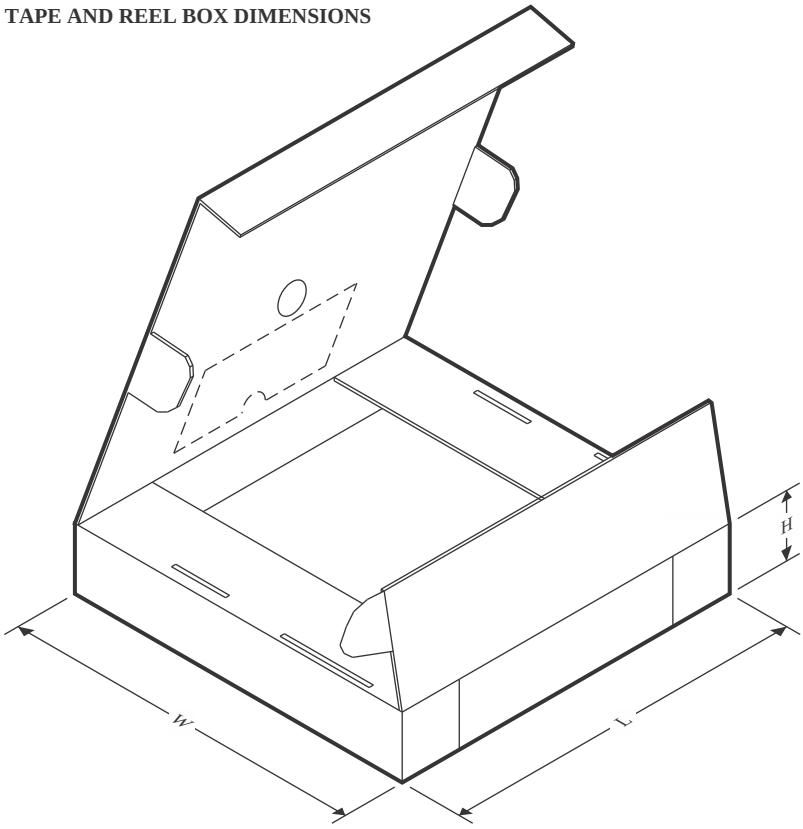
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA826AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA826AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA826AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA826AIDRGRG4	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA826AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

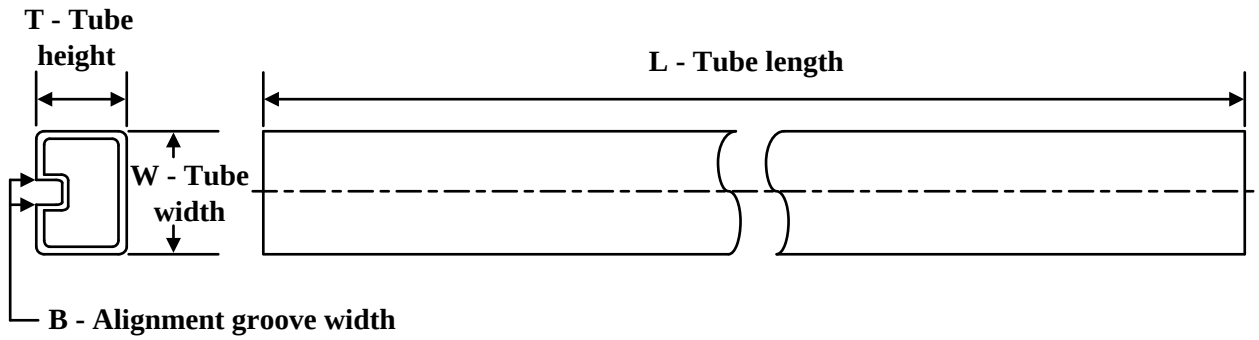
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA826AIDGKR	VSSOP	DGK	8	2500	346.0	346.0	41.0
INA826AIDGKRG4	VSSOP	DGK	8	2500	346.0	346.0	41.0
INA826AIDRGR	SON	DRG	8	3000	346.0	346.0	33.0
INA826AIDRGRG4	SON	DRG	8	3000	346.0	346.0	33.0
INA826AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

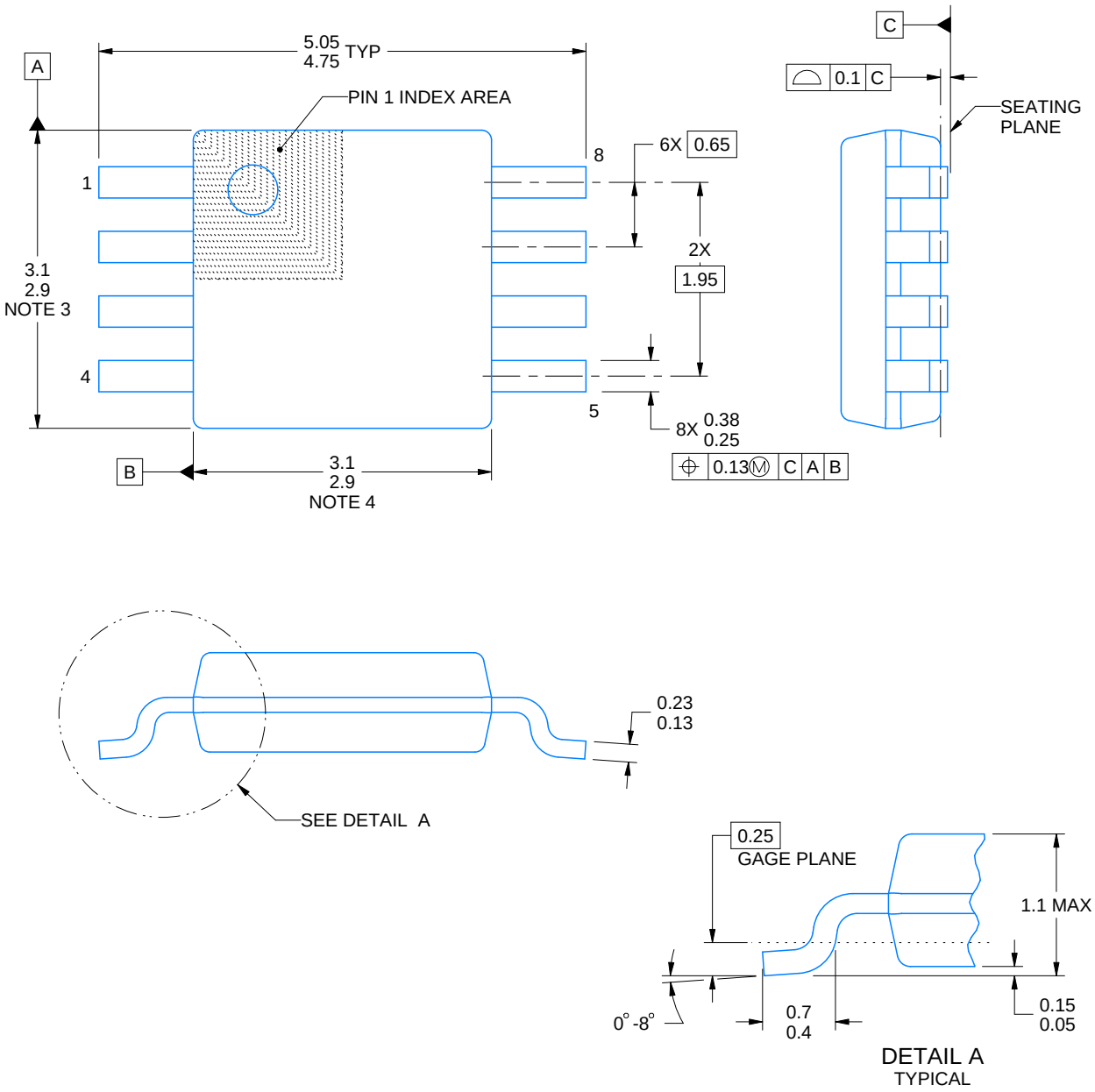
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA826AID	D	SOIC	8	75	506.6	8	3940	4.32
INA826AID.B	D	SOIC	8	75	506.6	8	3940	4.32
INA826AIDGK	DGK	VSSOP	8	80	274	6.2	2540	2.5
INA826AIDGK.B	DGK	VSSOP	8	80	274	6.2	2540	2.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

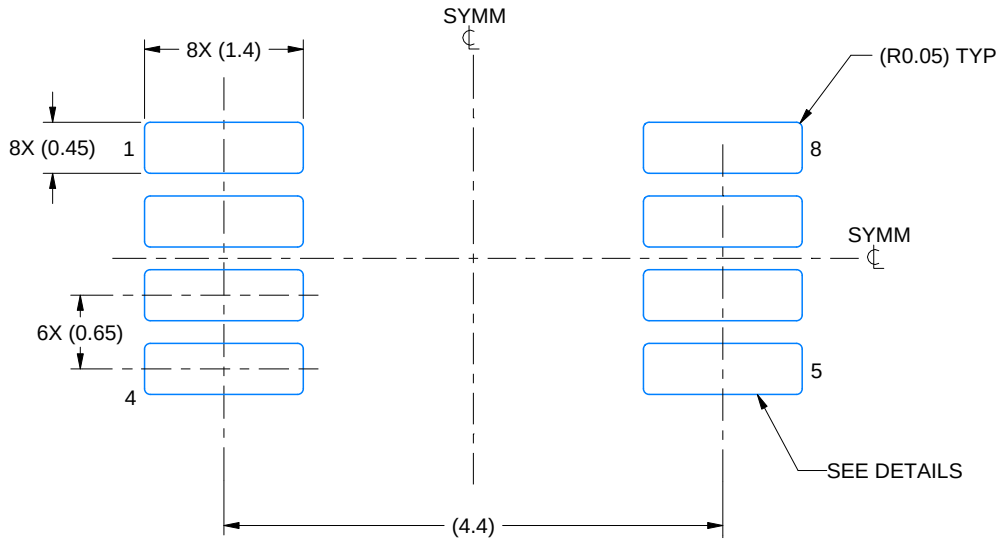
SMALL OUTLINE PACKAGE



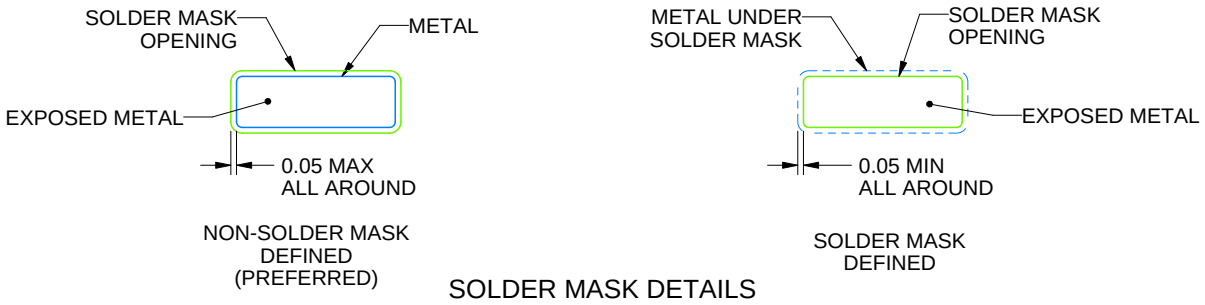
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

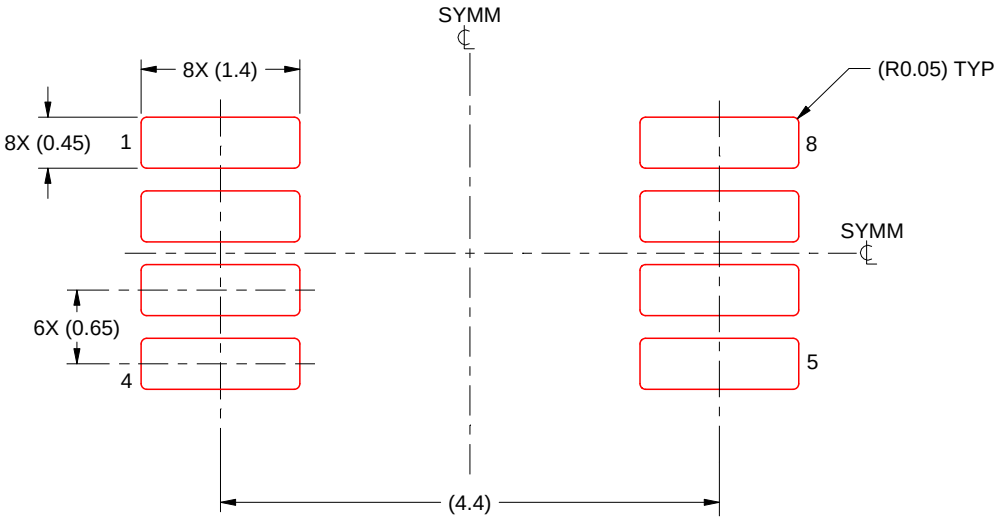


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

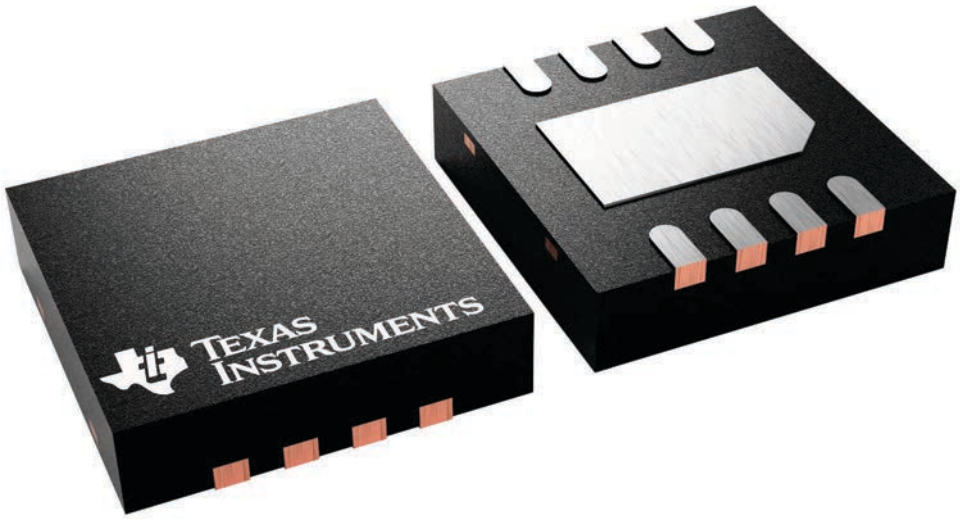
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



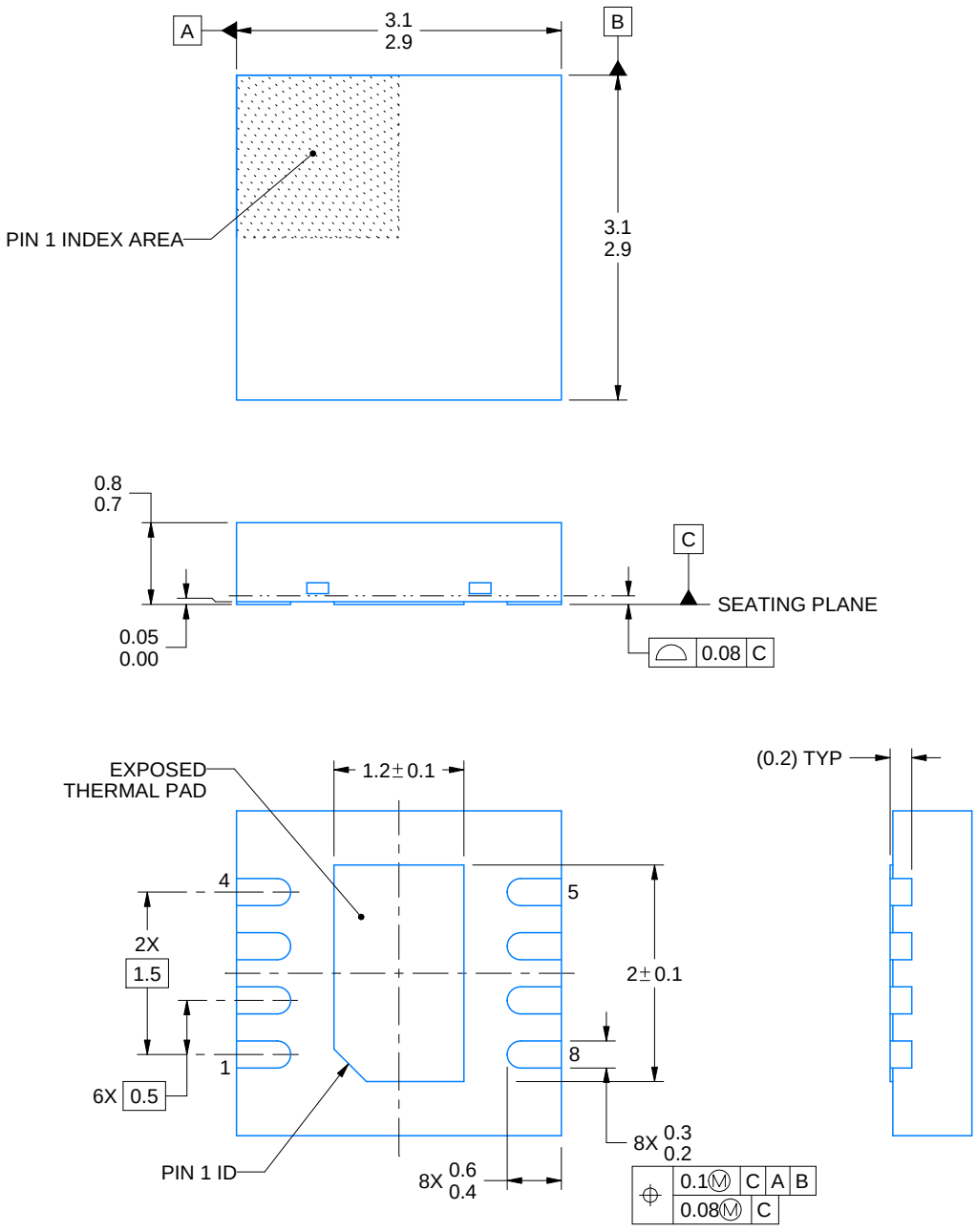
4225794/A

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

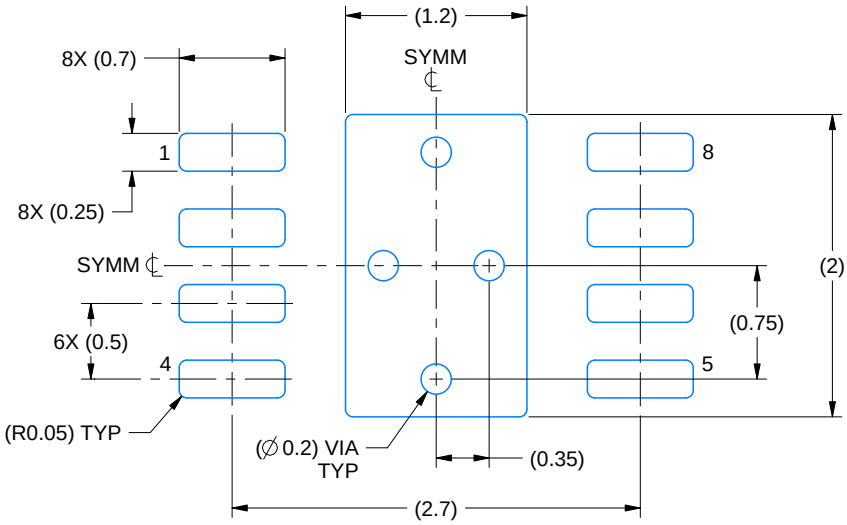
PLASTIC SMALL OUTLINE - NO LEAD



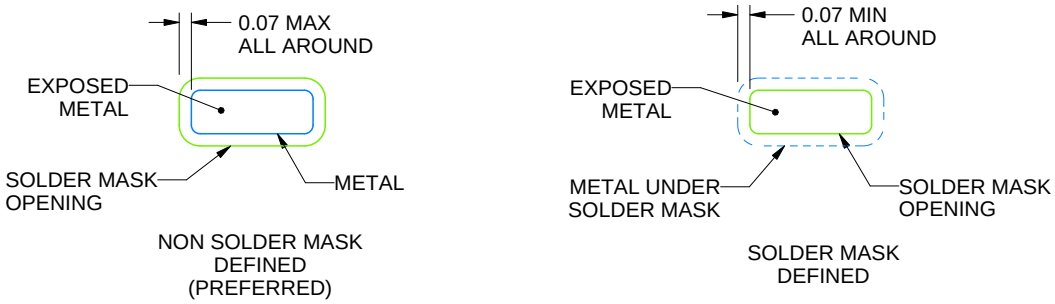
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

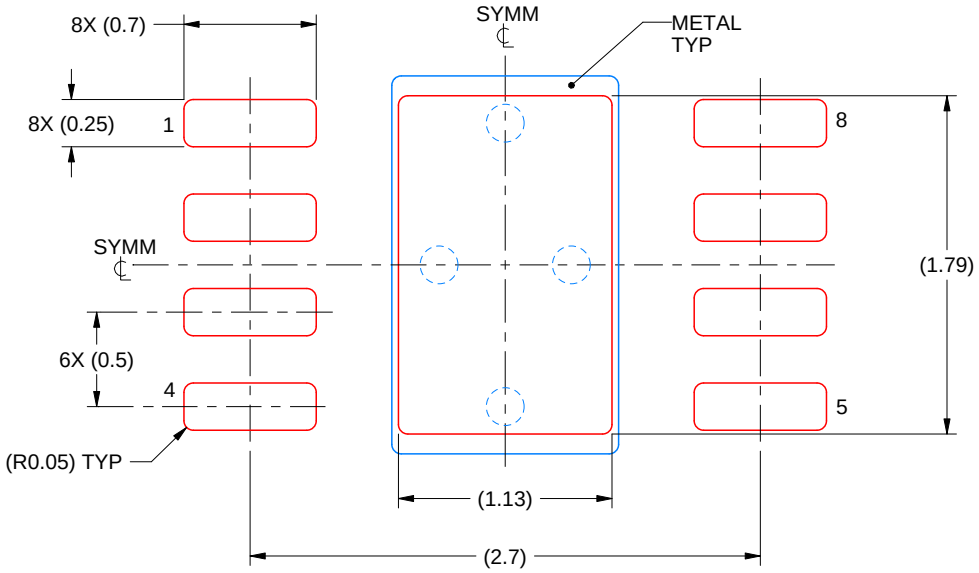


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



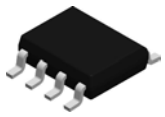
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

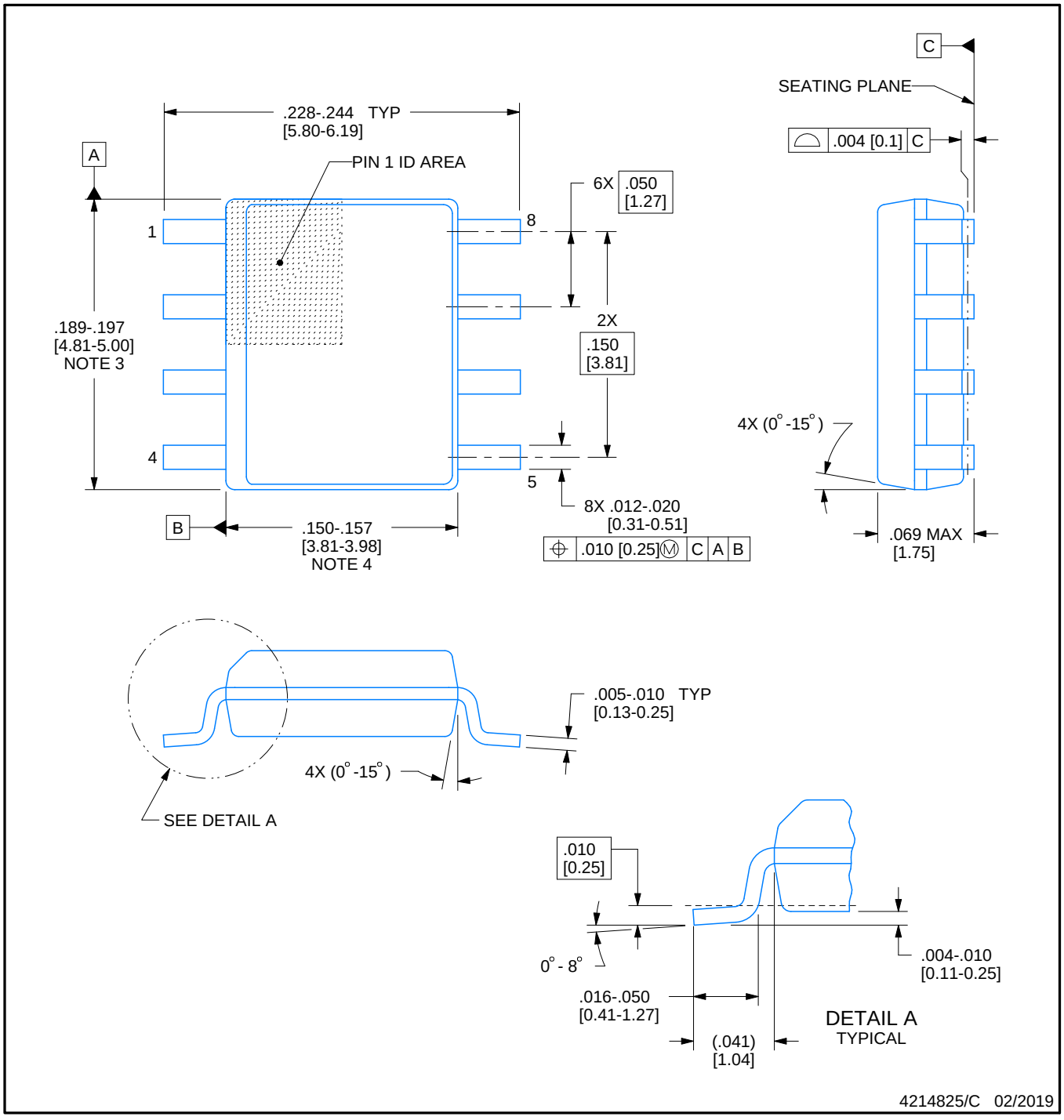


PACKAGE OUTLINE

D0008A

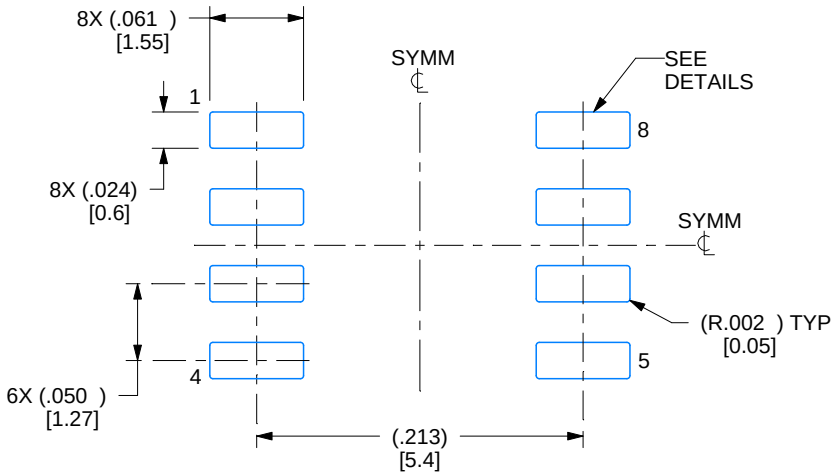
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

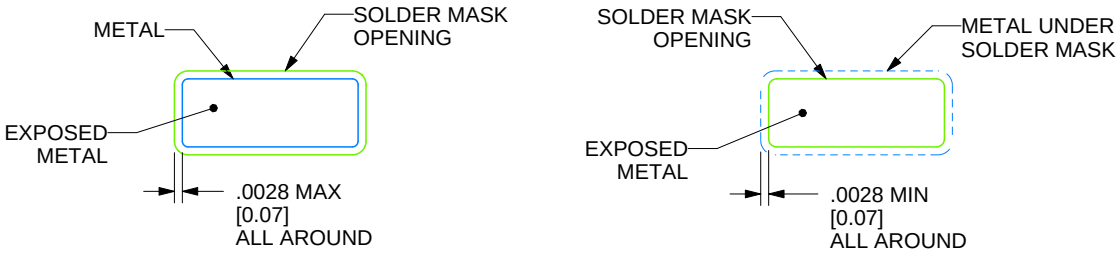


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

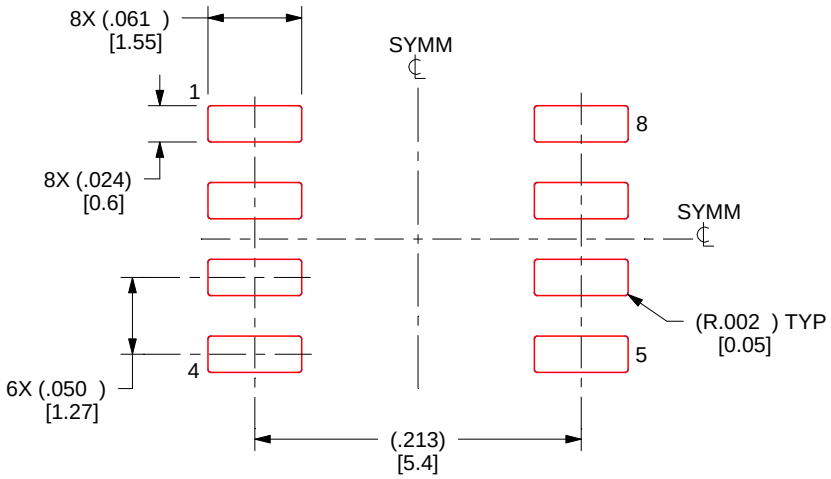
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025