

PE64907

Product Specification

UltraCMOS® Digitally Tunable Capacitor, 100–3000 MHz



Features

- 3-wire SPI-compatible serial interface with built-in bias voltage generation and ESD protection
- 5-bit, 32-state digitally tunable capacitor
- Shunt configuration $C = 0.85 \text{ pF}$ to 2.4 pF (2.82:1 tuning ratio) in discrete 50 fF steps
- High RF power handling: 30 V_{PK}
- High linearity
- Wide power supply range: 2.3–4.8V
- Low current consumption: 140 μA at 2.75V typ.
- High ESD tolerance: 2-kV HBM on all pins
- Packaging: 10-lead $2 \times 2 \times 0.55 \text{ mm}$ QFN

Applications

- Tunable antennas
- Tunable matching networks
- Tunable filter networks

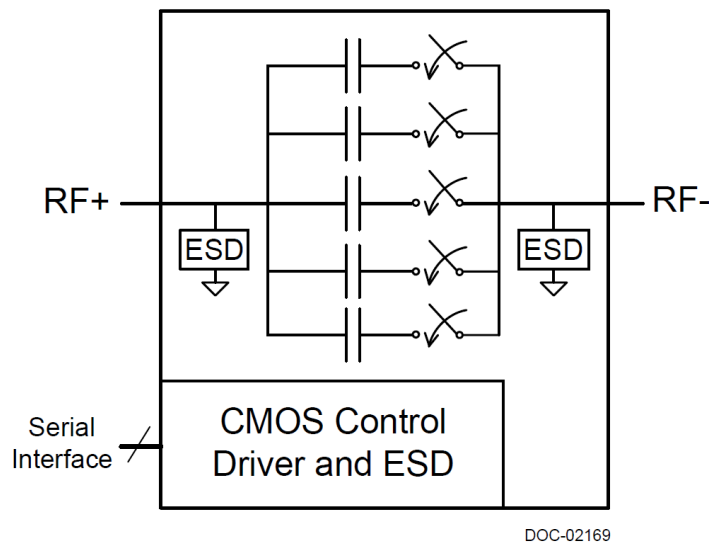


Figure 1. PE64907 functional diagram

Product description

The PE64907 is a DuNE™ technology enhanced digitally tunable capacitor (DTC) based on pSemi's UltraCMOS® technology. This highly versatile product supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications.

The PE64907 offers high RF power handling and ruggedness while meeting challenging harmonic and linearity requirements enabled by pSemi's HaRP™ technology. The device is controlled through the widely supported 3-wire SPI-compatible interface. All decoding and biasing are integrated on-chip, and no external bypassing or filtering components are required.

DuNE™ devices feature ease of use while delivering superior RF performance in the form of tuning accuracy, monotonicity, tuning ratio, power handling, size, and quality factor. With built-in bias voltage generation and ESD protection, DTC products provide a monolithically integrated tuning solution for demanding RF applications.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
ESD Voltage HBM ^(*)	V _{ESD}	–	2000	V
Note: * Human Body Model (MIL-STD-883 Method 3015.7)				

Recommended operating conditions

Table 2 lists the PE64907 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.30	2.75	4.80	V
Supply current, $V_{DD} = 2.75V$	I_{DD}	–	140	200	μA
Standby current, $V_{DD} = 2.75V$	I_{DD}	–	25	–	μA
Control voltage high	V_{IH}	1.2	1.8	3.1	V
Control voltage low	V_{IL}	0	0	0.57	V
RF input power, 50 Ω : ⁽¹⁾ - 698–915 MHz - 1710–1910 MHz	–	–	–	+34 +32	dBm
Peak operating RF voltage: ⁽²⁾ - VP to VM - VP to RFGND	–	–	–	30 30	V_{PK}
Operating temperature range	T_{OP}	–40	+25	+85	°C
Storage temperature range	T_{ST}	–65	+25	+150	°C

- Notes:
1. The maximum power available from a 50 Ω source. Pulsed RF input with 4620- μ S period, 50% duty cycle, measured per 3GPP TS 45.005 measured in shunt between 50 Ω ports, with RF- connected to GND.
 2. Node voltages defined per the equivalent circuit model schematic in [Figure 10](#). When the DTC is used as a part of reactive network, impedance transformation could cause the internal RF voltages (V_P and V_M in [Figure 10](#)) to exceed the peak operating RF voltage even with the specified RF input power levels. For operations above +20 dBm (100 mW), the complete RF circuit must be simulated using actual input power and load conditions, and internal node voltages V_P and V_M monitored to not exceed 30 V_{PK} .

Electrical specifications

Table 3 lists the PE64907 key electrical specifications at 25 °C and $V_{DD} = 2.75V$ in shunt configuration with RF- connected to ground, unless otherwise specified.

Table 3. Electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency	–	100	–	3000	MHz
Minimum capacitance, C_{MIN}	State 00000, 100 MHz	0.68	0.85	1.02	pF
Maximum capacitance, C_{MAX}	State 11111, 100 MHz	1.92	2.40	2.88	pF
Tuning ratio	C_{MAX}/C_{MIN} , 100 MHz	–	2.82:1	–	–
Step size	5 bits (32 states), 100 MHz	–	0.050	–	pF
Quality factor at $C_{MIN}^{(1)}$	698–960 MHz, with L_S removed 1710–2170 MHz, with L_S removed	–	41 37	–	–
Quality factor at $C_{MAX}^{(1)}$	698–960 MHz, with L_S removed 1710–2170 MHz, with L_S removed	–	34 16	–	–
Self-resonant frequency	State 00000 State 11111	–	8.3 3.5	–	GHz
Harmonics ⁽²⁾	2fo, 3fo: 698–915 MHz; $P_{IN} +34$ dBm, 50Ω 2fo, 3fo: 1710–1910 MHz; $P_{IN} +32$ dBm, 50Ω	–	–	-36 -36	dBm
IMD3	Bands I, II, V/VIII, +20 dBm CW at Tx freq, -15 dBm CW at 2Tx-Rx freq, 50Ω	–	–	-105	dBm
Third-order intercept point, IP3	Shunt configuration derived from IMD3 spec $IP3 = (2P_{TX} + P_{BLOCK} - IMD3)/2$	–	65	–	dBm
Switching time ⁽³⁾⁽⁴⁾	State change to 10/90% delta capacitance between any two states	–	–	12	μs
Start-up time ⁽³⁾	Time from V_{DD} within specification to all performances within specification	–	–	70	μs
Wake-up time ⁽³⁾⁽⁴⁾	State change from standby mode to RF state to all performances within specification	–	–	70	μs

Notes:

- The Q for a shunt DTC is based on a series RLC equivalent circuit:
 $Q = X_C / R = (X - X_L) / R$, where $X = X_L + X_C$, $X_L = 2 \times \pi \times f \times L$, and $X_C = -1 / (2 \times \pi \times f \times C)$,
 which is equivalent to removing the effect of parasitic inductance L_S .
- In shunt between 50Ω ports. Pulsed RF input with 4620-μs period, 50% duty cycle, measured per 3GPP TS 45.005.
- To achieve the specified performance, provide a DC path to ground at RF.
- The state change is activated on the falling edge of SEN following the data word.

Typical performance data

Figure 2–Figure 7 show the typical performance data at +25 °C and $V_{DD} = 2.75V$, unless otherwise specified.

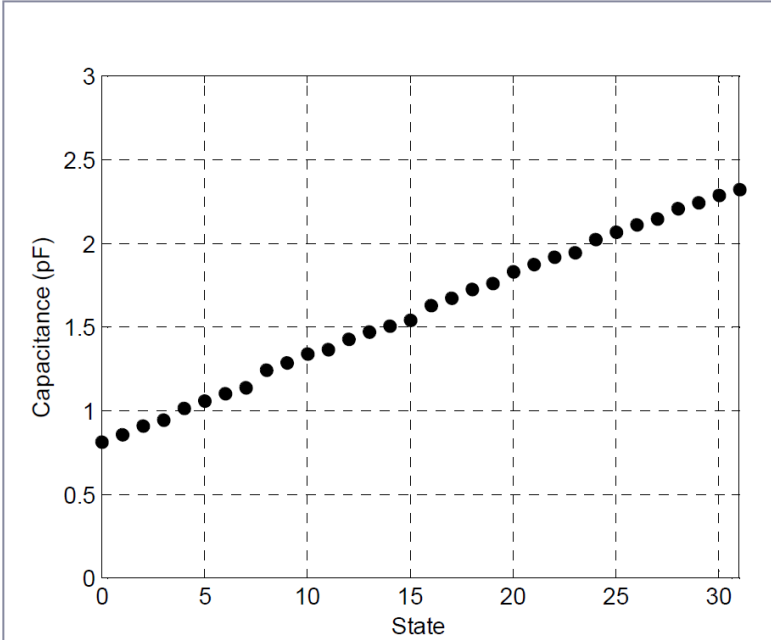


Figure 2. Measured shunt C (at 100 MHz) vs. state

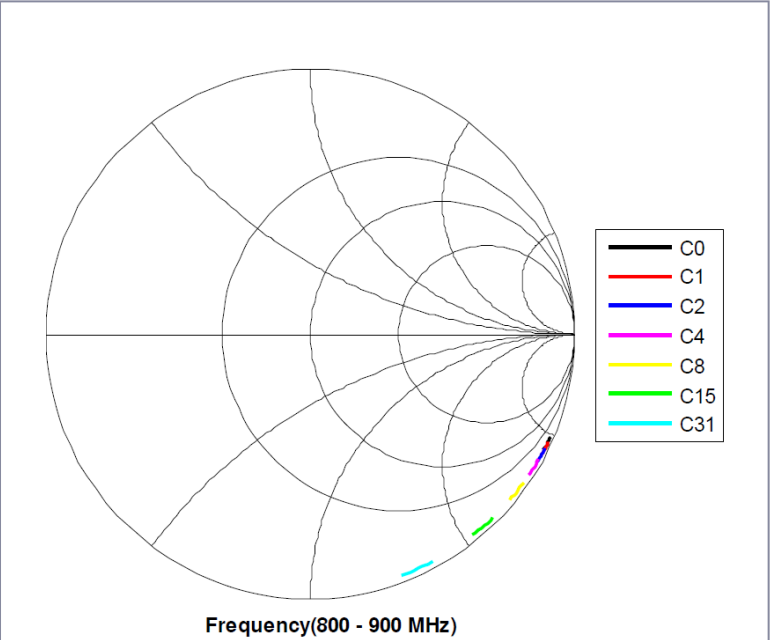


Figure 3. Measured shunt S_{11} (major states)

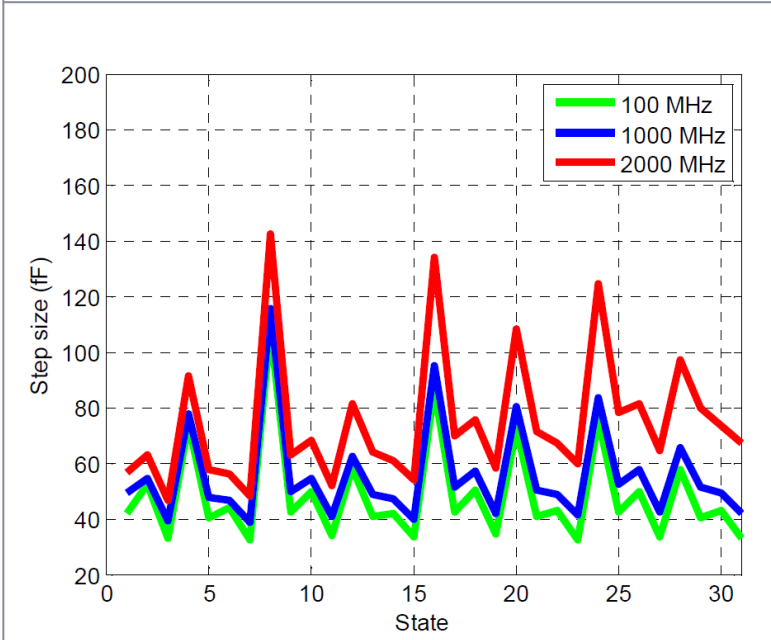


Figure 4. Measured step size vs. state (frequency)

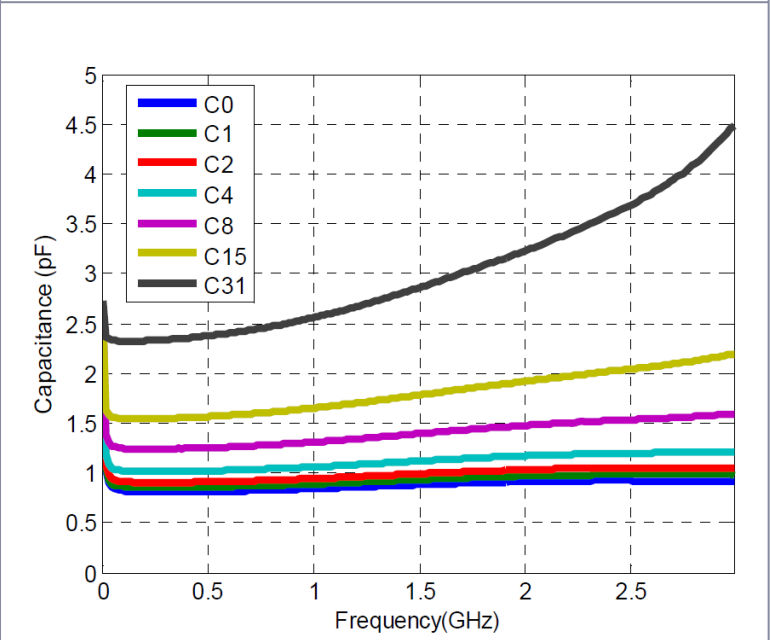
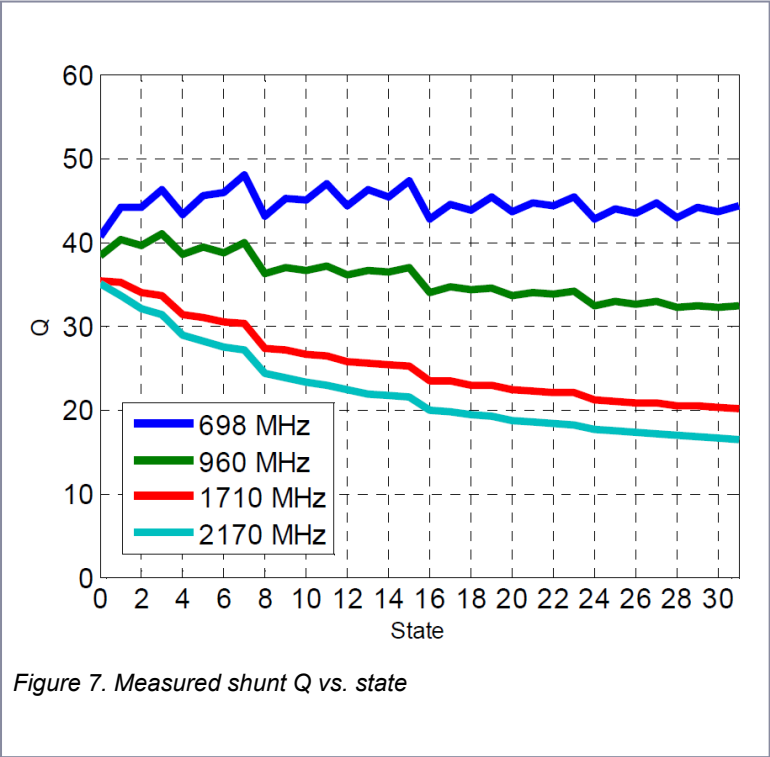
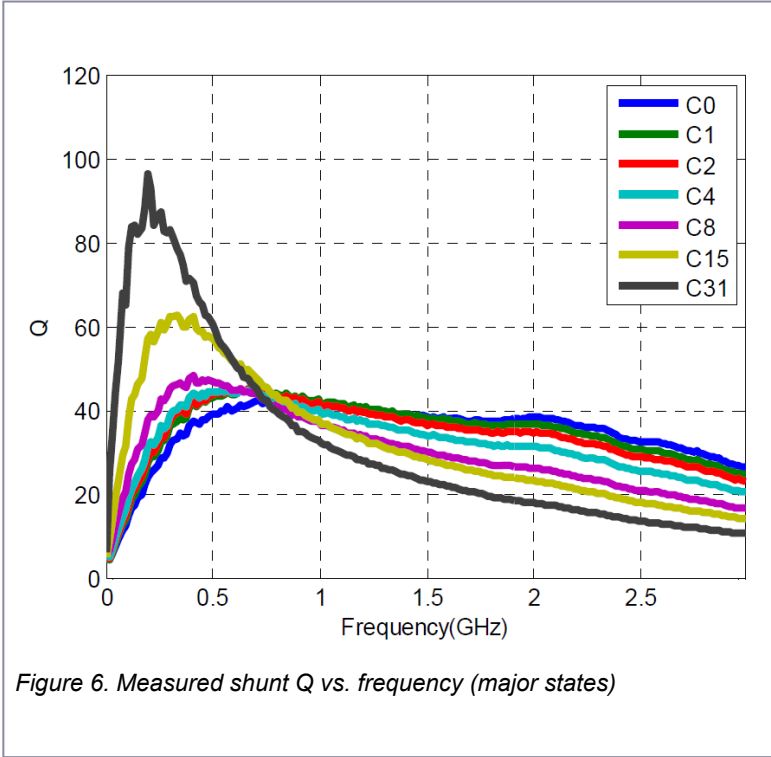


Figure 5. Measured shunt C vs. frequency (major states)



Serial interface operation and sharing

The PE64907 is controlled by a 3-wire SPI-compatible interface with enable active high. As shown in Figure 8, the serial master initiates the start of a telegram by driving the Serial Enable (SEN) line high. Each bit of the 8-bit telegram (MSB first in) is clocked in on the rising edge of the Serial Clock (SCL), as shown in Figure 8 and Table 4. Transitions on Serial Data (SDA) are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last eight bits it received.

More than one DTC can be controlled by one interface using a dedicated SEN line for each DTC. The SDA, SCL, and VDD lines can be shared, as shown in Figure 9. Dedicated SEN lines act as a chip select so that each DTC only responds to the serial transactions intended for them. This makes each DTC change states sequentially as they are programmed.

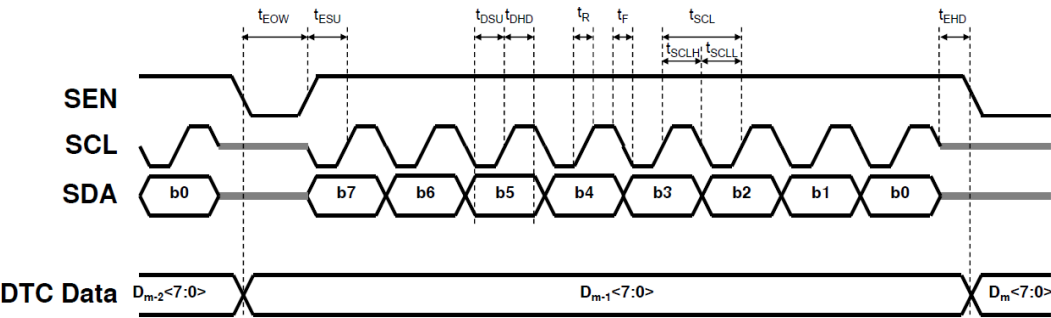


Figure 8. Serial interface timing diagram

Table 4. 8-bit serial programming register map

b7	b6	b5	b4	b3	b2	b1	b0
0 ⁽¹⁾	0 ⁽¹⁾	STB ⁽²⁾	d4	d3	d2	d1	d0
↑ MSB (first in)	—						↑ LSB (last in)
Notes: 1. These bits are reserved and must be written to 0 for proper operation. 2. The DTC is active when low (set to 0), and in low-current standby mode when high (set to 1).							

Table 5 lists the serial interface timing characteristics at $V_{DD} = 2.75V$ and $-40\text{ }^{\circ}C < T_A < +85\text{ }^{\circ}C$, unless otherwise specified.

Table 5. Serial interface timing characteristics

Parameter	Symbol	Min	Max	Unit
Serial clock period	t_{SCL}	38.4	–	ns
SCL low time	t_{SCLL}	13.2	–	ns
SCL high time	t_{SCLH}	13.2	–	ns
SCL, SDA, SEN rise time	t_R	–	6.5	ns
SCL, SDA, SEN fall time	t_F	–	6.5	ns
SEN rising edge to SCL rising edge	t_{ESU}	19.2	–	ns
SCL rising edge to SEN falling edge	t_{EHD}	19.2	–	ns
SDA valid to SCL rising edge	t_{DSU}	13.2	–	ns
SDA valid after SCL rising edge	t_{DHD}	13.2	–	ns
SEN falling edge to SEN rising edge	t_{EOW}	38.4	–	ns

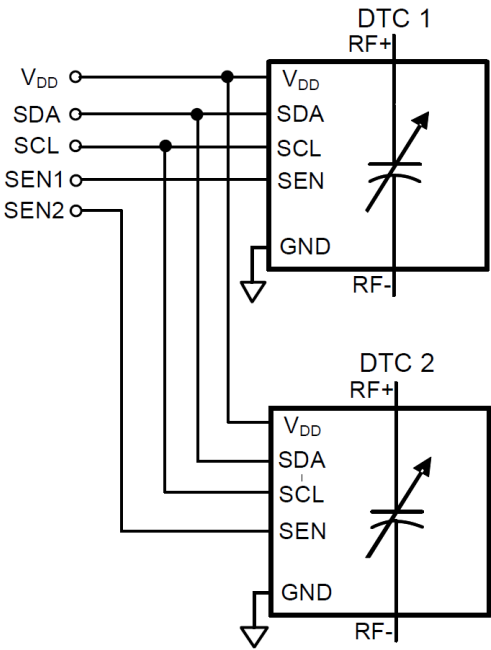


Figure 9. Recommended bus sharing

Equivalent circuit model description

The DTC equivalent circuit model includes all parasitic elements and is accurate in both series and shunt configurations, reflecting physical circuit behavior accurately and providing close correlation to measured data. It can easily be used in circuit simulation programs.

For the V_P and V_M maximum operating limits, see [Table 2](#).

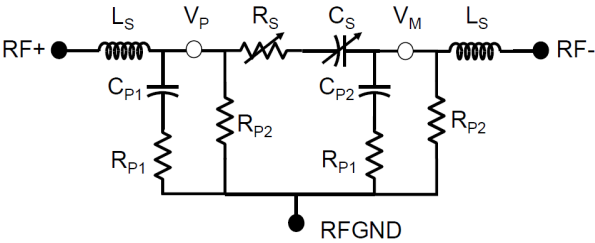


Figure 10. Equivalent circuit model schematic

Table 6. Equivalent circuit model parameters

Variable	Equation (state = 0, 1, 2...31)	Unit
C _S	0.056 × state + 0.38	pF
R _S	20 / (state + 20 / (state + 0.7)) + 0.7	Ω
R _{P1}	8 + state	Ω
R _{P2}	25000 + 3 × state^3	Ω
C _{P1}	-0.0061 × state + 0.47	pF
C _{P2}	0.0096 × state + 0.61	pF
L _S	0.35	nH

Table 7. Equivalent circuit data

State			DTC core		Parasitic elements	
Hex	Bin	Dec	C _S (pF)	R _S (Ω)	C _{P1}	C _{P2}
0x00	00000	0	0.38	1.40	0.47	0.61
0x01	00001	1	0.44	2.27	0.46	0.62
0x02	00010	2	0.49	2.83	0.46	0.63
0x03	00011	3	0.55	3.08	0.45	0.64
0x04	00100	4	0.60	3.12	0.45	0.65
0x05	00101	5	0.66	3.05	0.44	0.66
0x06	00110	6	0.72	2.93	0.43	0.67
0x07	00111	7	0.77	2.78	0.43	0.68

Table 7. Equivalent circuit data, continued

State			DTC core		Parasitic elements	
Hex	Bin	Dec	C _S (pF)	R _S (Ω)	C _{P1}	C _{P2}
0x08	01000	8	0.83	2.64	0.42	0.69
0x09	01001	9	0.88	2.51	0.42	0.70
0x0A	01010	10	0.94	2.39	0.41	0.71
0x0B	01011	11	1.00	2.27	0.40	0.72
0x0C	01100	12	1.05	2.17	0.40	0.73
0x0D	01101	13	1.11	2.08	0.39	0.73
0x0E	01110	14	1.16	2.00	0.38	0.74
0x0F	01111	15	1.22	1.93	0.38	0.75
0x10	10000	16	1.28	1.86	0.37	0.76
0x11	10001	17	1.33	1.80	0.37	0.77
0x12	10010	18	1.39	1.76	0.36	0.78
0x13	10011	19	1.44	1.70	0.35	0.79
0x14	10100	20	1.50	1.65	0.35	0.80
0x15	10101	21	1.56	1.61	0.34	0.81
0x16	10110	22	1.61	1.57	0.34	0.82
0x17	10111	23	1.67	1.54	0.33	0.83
0x18	11000	24	1.72	1.51	0.32	0.84
0x19	11001	25	1.78	1.48	0.32	0.85
0x1A	11010	26	1.84	1.45	0.31	0.86
0x1B	11011	27	1.89	1.42	0.31	0.87
0x1C	11100	28	1.95	1.40	0.30	0.88
0x1D	11101	29	2.00	1.37	0.29	0.89
0x1E	11110	30	2.06	1.35	0.29	0.90
0x1F	11111	31	2.12	1.33	0.28	0.91

Series operation

In series configuration, the effective capacitance between the RF+ and RF- ports is represented by C_S and the tuning ratio as C_{Smax}/C_{Smin} .

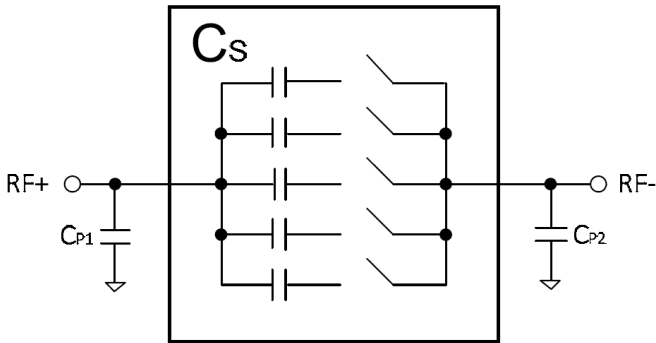


Figure 11. Effective capacitance diagram

The shunt configuration—looking into RF+ when RF- is grounded—has a higher total capacitance at RF+ due to the parallel combination of C_S with parasitic capacitance C_{P1} ($C_S + C_{P1}$), as shown in Figure 12 and Table 8.

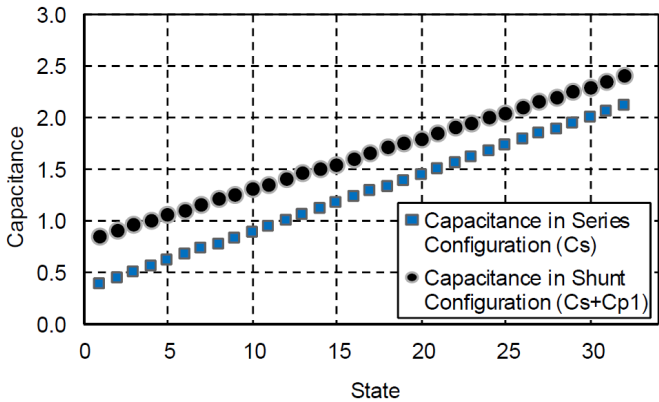
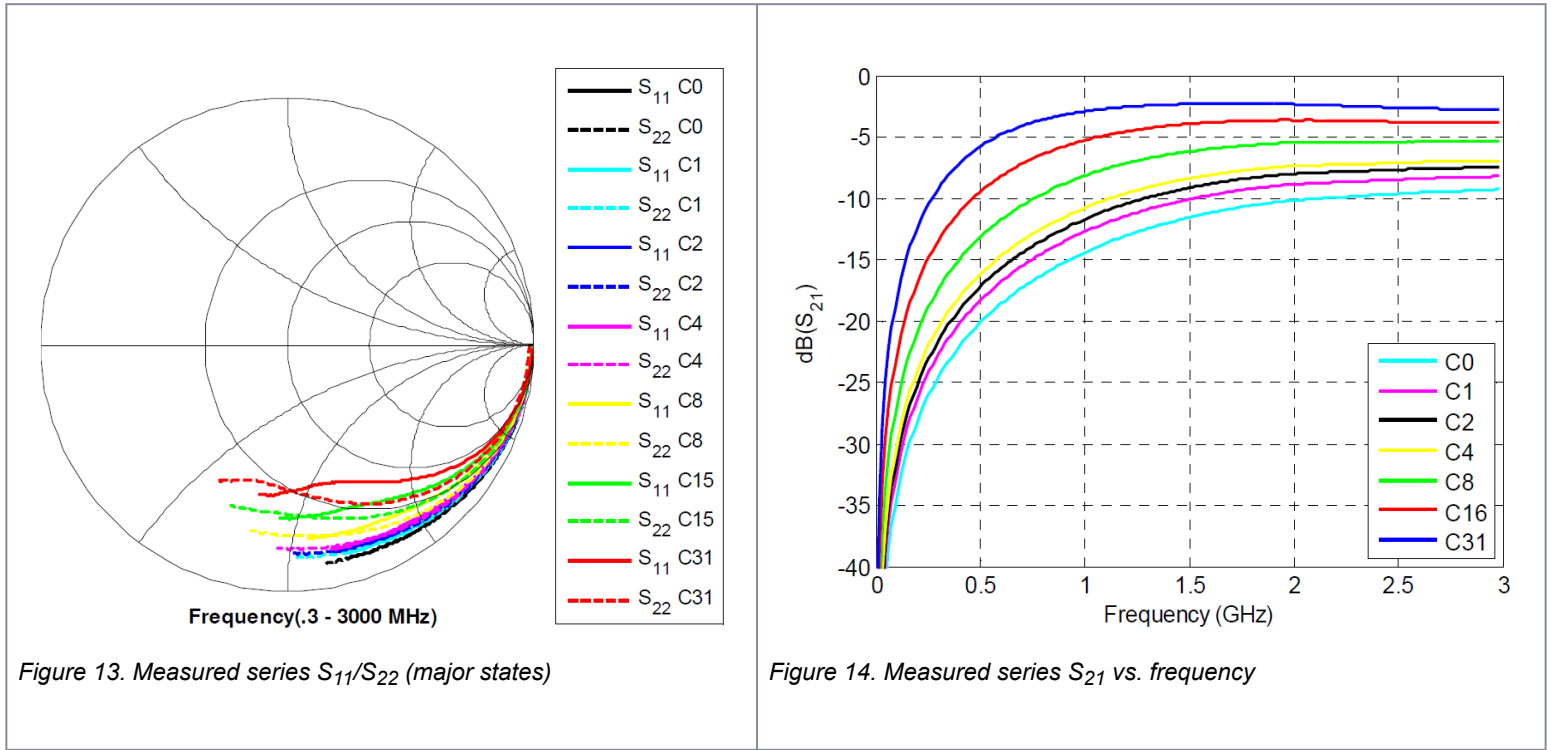


Figure 12. Typical capacitance vs. state

Table 8. Effective capacitance summary

Configuration	Effective capacitance	C_{MIN} (state 0)	C_{MAX} (state 31)	Tuning ratio
Series (RF+ to RF-)	C_S	0.38	2.12	5.58:1
Shunt (RF+ to GND)	$C_S + C_{P1}$	0.85	2.4	2.82:1

Figure 13 and Figure 14 show S_{11} and S_{21} for the series configuration, respectively. S_{21} includes mismatch and dissipative losses and is not indicative of tuning network loss. Use the equivalent circuit model to simulate tuning network loss.



When the DTC is used as a part of a reactive network, impedance transformation can cause the internal RF voltages (V_P and V_M in Figure 10) to exceed peak operating RF voltage. The complete RF circuit must be simulated using actual input power and load conditions to ensure that neither V_P nor V_M exceed $30 V_{PK}$.

Layout recommendations

For optimal results, place a ground fill directly under the DTC package on the PCB. Layout isolation is between all control and RF lines is important. When using the DTC in a shunt configuration, ensure that the RF- pin is solidly grounded to a filled ground plane. Make ground traces as short as possible to minimize inductance. A continuous ground plane is preferred on the top layer of the PCB. When using multiple DTCs together, minimize the physical distance between them and make the connection as wide as possible to minimize the series parasitic inductance.

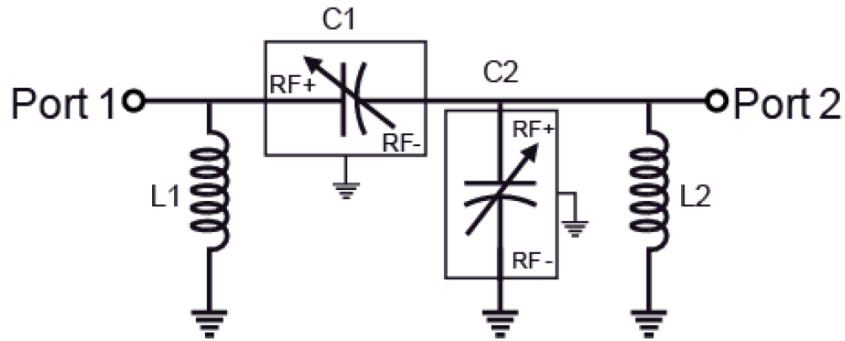


Figure 15. Recommended schematic of multiple DTCs

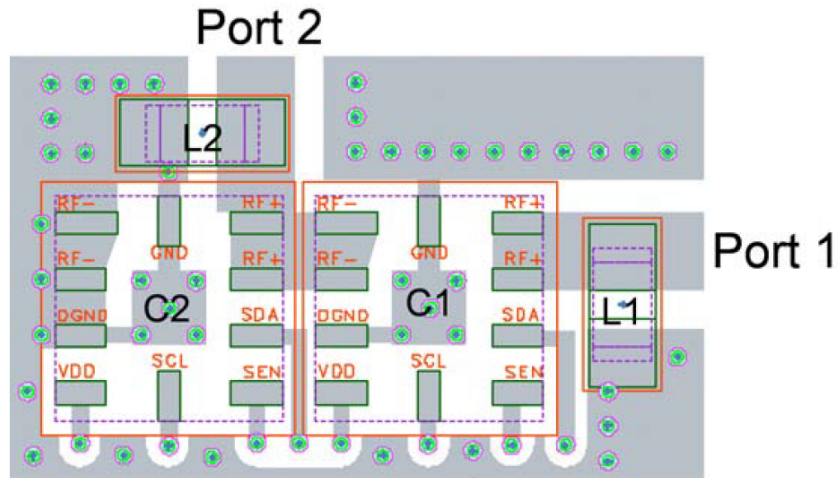


Figure 16. Recommended layout of multiple DTCs

Evaluation board

pSemi designed the 101-0675 evaluation board (EVB) to accurately measure the DTC impedance and loss. Two configurations are available: 1-port shunt (J3), and 2-port shunt (J4, J5). Three calibration standards are provided. The open (J2) and short (J1) standards (104-ps delay) are used to perform port extensions and account for electrical length and transmission line loss. The Thru (J9, J10) standard can be used to estimate PCB transmission line losses for scalar de-embedding of the 2-port series configuration (J4, J5).

The board consists of a 4-layer stack with two outer layers made of Rogers 4350B ($\epsilon_r = 3.48$) and two inner layers of FR4 ($\epsilon_r = 4.80$). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

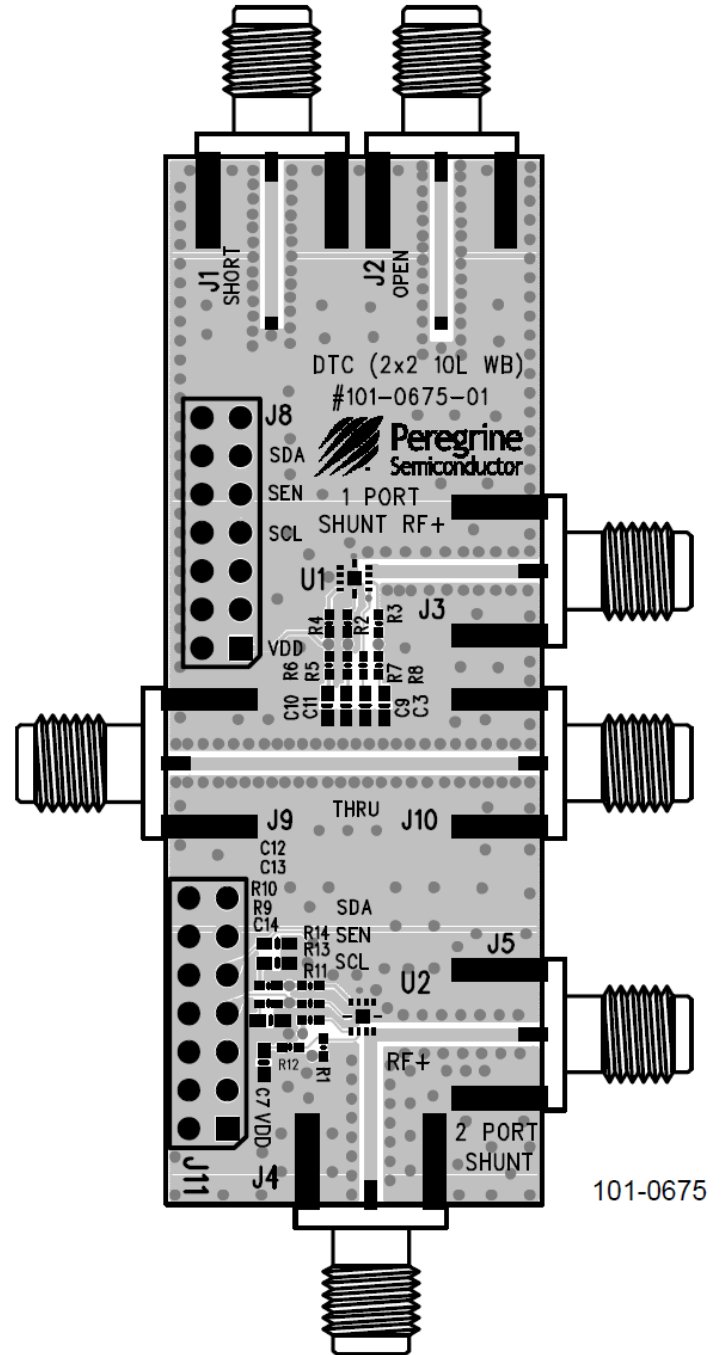


Figure 17. Evaluation board layout

Pin configuration

Figure 18 shows the PE64907 pin configuration for the 10-lead $2 \times 2 \times 0.55$ mm QFN package, and Table 9 lists the description for each pin.

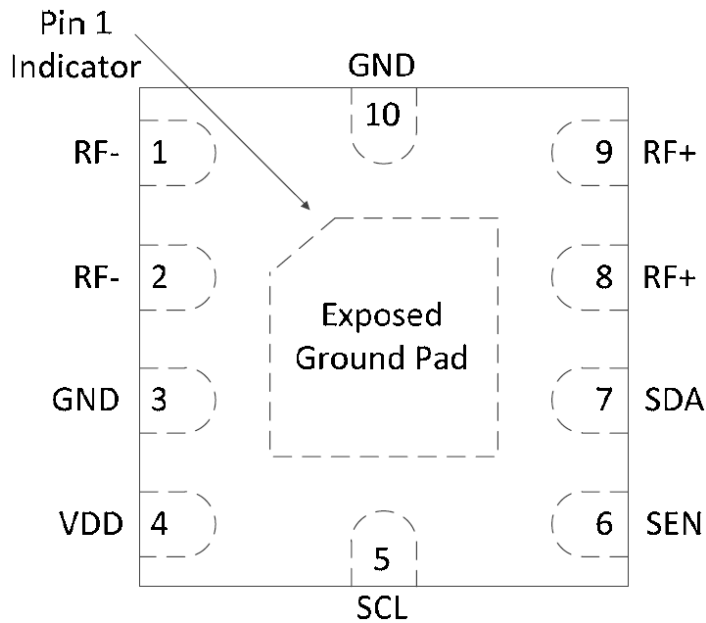


Figure 18. Pin configuration, top view

Table 9. Pin descriptions

Pin no.	Pin name	Description
1	RF- ⁽¹⁾	Negative RF port
2	RF- ⁽¹⁾	Negative RF port
3, 10	GND ⁽²⁾	Ground
4	V _{DD}	Power supply
5	SCL	Serial interface clock input
6	SEN	Serial interface latch enable input
7	SDA	Serial interface data input
8	RF+ ⁽¹⁾	Positive RF port
9	RF+ ⁽¹⁾	Positive RF port
PAD	GND ⁽²⁾	Exposed pad. Ground for proper operation.

- Notes:
- For optimal performance, tie Pins 1–2 and Pins 8–9 together on the PCB.
 - For optimal performance, tie Pins 3, 10, and the exposed ground pad together on the PCB.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
 - Package drawing
- Package marking
 - Tape-and-reel information

Moisture sensitivity level

The PE64907 moisture sensitivity level rating for the 10-lead 2 × 2 × 0.55 mm QFN package is MSL1.

Package drawing

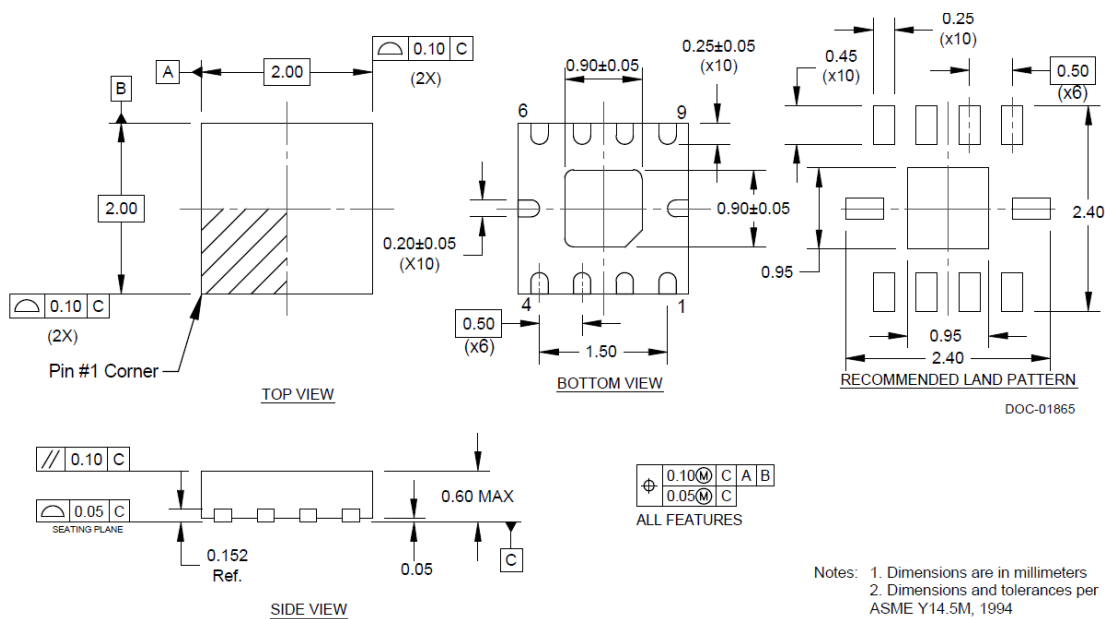


Figure 19. Package mechanical drawing for the 10-lead 2 × 2 × 0.55 mm QFN package

Top-marking specification

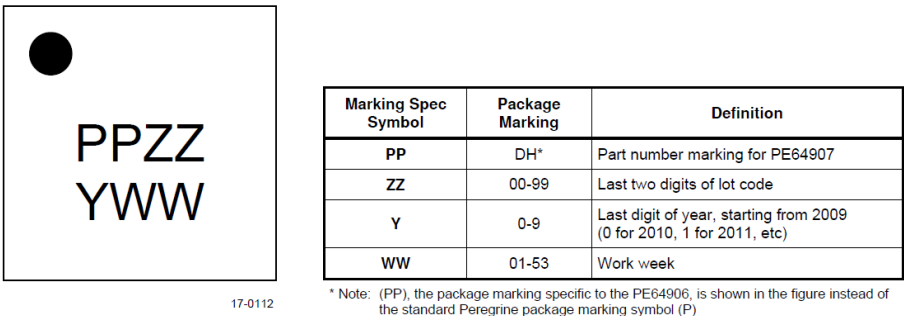


Figure 20. Package marking specification

Tape and reel specification

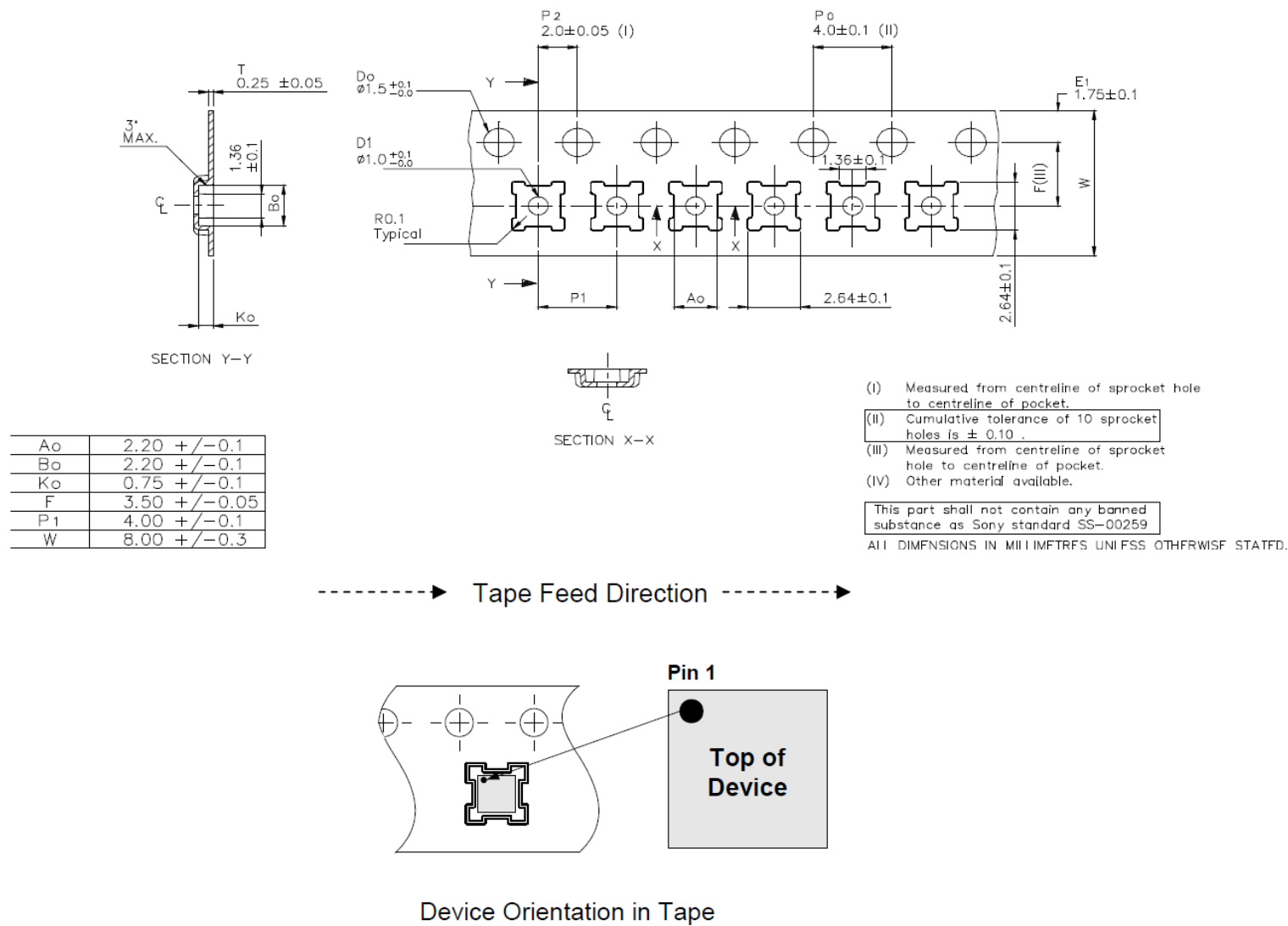


Figure 21. Tape and reel specification for the 10-lead 2 × 2 × 0.55 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE64907	PE64907 digitally tunable capacitor	Green 10-lead 2 × 2 × 0.55 mm QFN	3000 units/T&R
EK64907-01	PE64907 evaluation kit	Evaluation kit	1/box

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