

PE64904

Product Specification

UltraCMOS® Digitally Tunable Capacitor (DTC), 100–3000 MHz



Features

- 3-wire (SPI compatible) serial interface with built-in bias voltage generation and ESD protection
- DuNE™-enhanced UltraCMOS® device
- 5-bit, 32-state digitally tunable capacitor
- Series configuration: $C = 0.60\text{--}4.60\text{ pF}$ (7.7:1 tuning ratio) in discrete 129-fF steps
- Shunt configuration: $C = 1.14\text{--}5.10\text{ pF}$ (4.6:1 tuning ratio) in discrete 129-fF steps
- High RF power handling up to 38 dBm, 30 V_{PK} RF, and high linearity
- Wide power supply range (2.3–3.6V) and low current consumption (typ. 140 μA at 2.6V)
- Excellent 1.5 kV HBM ESD tolerance on all pins
- Packaging: 10-lead $2 \times 2 \times 0.45\text{ mm}$ QFN

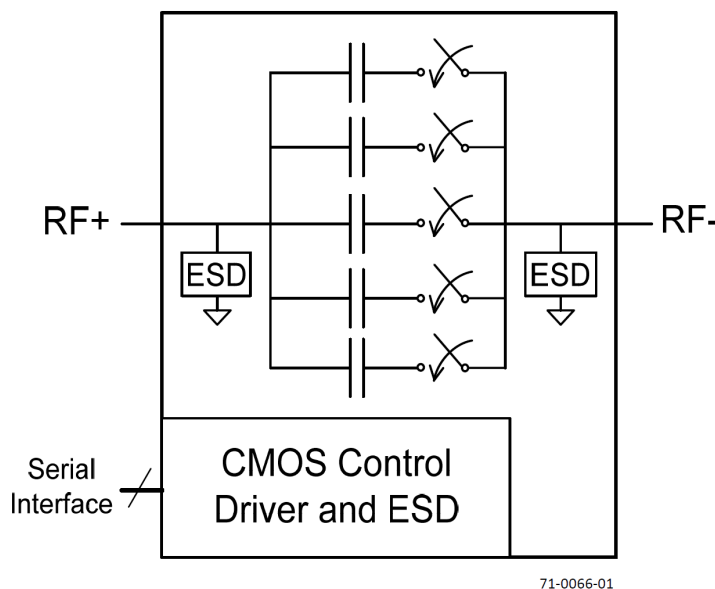


Figure 1. PE64904 functional diagram

Applications

- Tunable filter networks
- Tunable antennas
- RFID
- Tunable matching networks
- Phase shifters
- Wireless communications

Product description

The PE64904 is a DuNE™-enhanced digitally tunable capacitor (DTC) based on pSemi's UltraCMOS® technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications.

The PE64904 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements.

This highly versatile product can be used in series or shunt configurations to support a wide variety of tuning circuit topologies.

The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

pSemi's DuNE™ technology enables excellent linearity and exceptional harmonic performance. DuNE devices deliver performance superior to GaAs devices with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	-0.3	4.0	V
Voltage on any DC input	V_I	-0.3	4.0	V
ESD voltage HBM, all pins ⁽¹⁾	$V_{ESD,HBM}$	–	1500	V
ESD voltage CDM, all pins ⁽²⁾	$V_{ESD,CDM}$	–	750	V
Notes: 1. Human body model (MIL–STD 883 Method 3015.7) 2. Charged device model (JEDEC JESD22–C101)				

Recommended operating conditions

Table 2 lists the PE64904 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	2.6	3.6	V
Power supply current, $V_{DD} = 2.6V$	I_{DD}	–	140	200	μA
Standby current, $V_{DD} = 2.6V$	I_{DD}	–	25	–	μA
Control voltage high	V_{IH}	1.2	1.8	3.6	V
Control voltage low	V_{IL}	0	0	0.57	V
RF input power (50 Ω): ⁽¹⁾ - 698–915 MHz - 1710–1910 MHz	–	–	–	+34 +32	dBm
Peak operating RF voltage: ⁽²⁾ - V_P to V_M - V_P to RFGND - V_M to RFGND	–	–	–	30 30 30	V_{PK}
Operating temperature range	T_{OP}	-40	–	+85	°C
Storage temperature range	T_{ST}	-65	–	+150	°C

Notes:

- Maximum power available from 50 Ω source. Pulsed RF input with 4620- μS period, 50% duty cycle, measured per 3GPP TS 45.005.
- The node voltages are defined per the equivalent circuit model schematic ([Figure 16](#)). When the DTC is part of reactive network, impedance transformation can cause the internal RF voltages (V_P and V_M) to exceed the peak operating RF voltage even with the specified RF input power levels. For operation above +20 dBm (100 mW), the complete RF circuit must be simulated using actual input power and load conditions, and internal node voltages (V_P and V_M in [Figure 16](#)) monitored to not exceed 30 V_{PK} .

Electrical specifications

Table 3 lists the PE64904 key electrical specifications at +25 °C and $V_{DD} = 2.8V$, unless otherwise specified.

Table 3. Electrical specifications

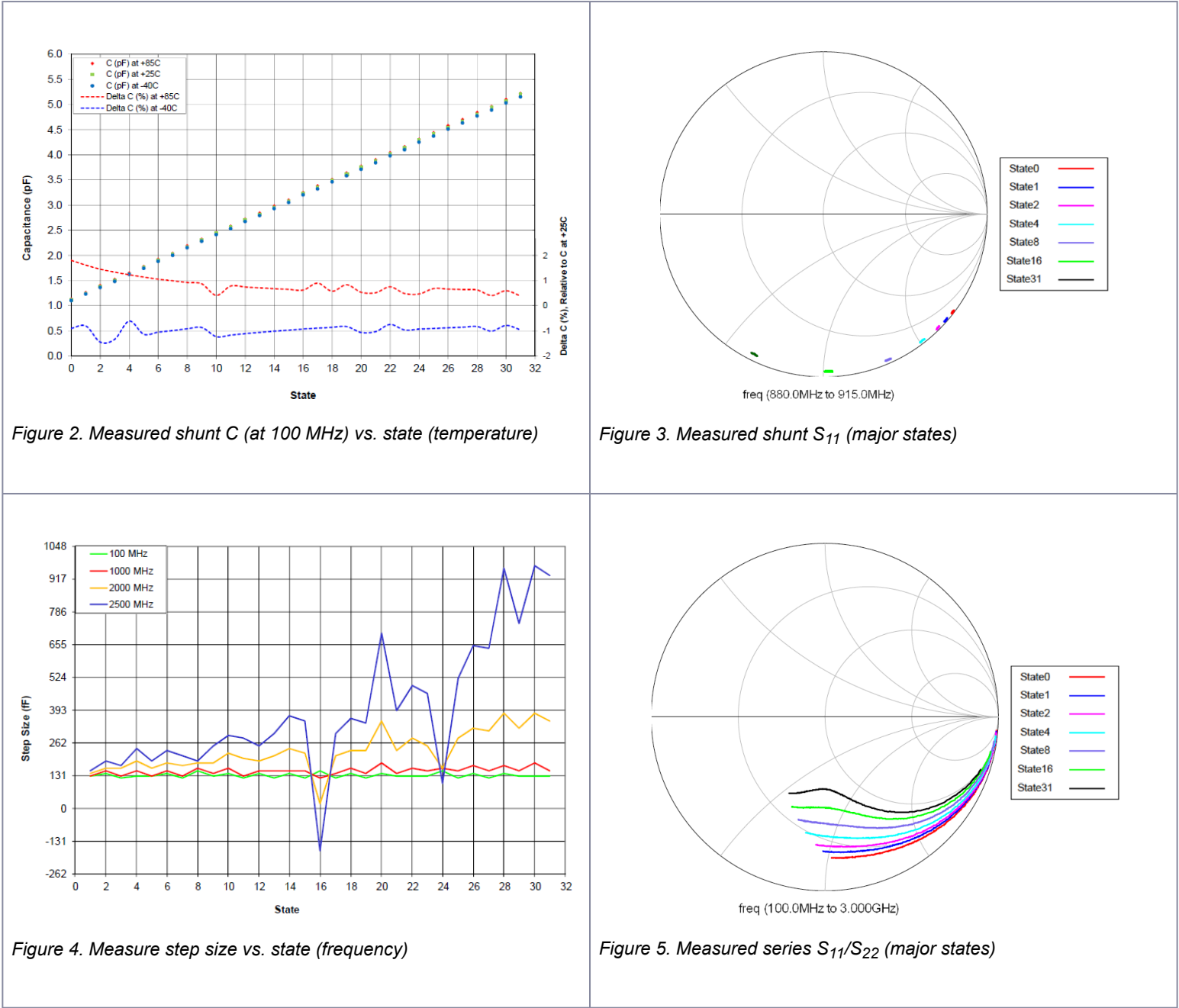
Parameter	Config.	Condition	Min	Typ	Max	Unit
Operating frequency	Both	–	100	–	3000	MHz
Minimum capacitance	Series	State = 00000, 100 MHz (RF+ to RF-)	0.49	0.60	0.71	pF
	Shunt	State = 00000, 100 MHz (RF+ to grounded RF-)	0.90	1.10	1.30	
Maximum capacitance	Series	State = 11111, 100 MHz (RF+ to RF-)	3.78	4.60	5.45	pF
	Shunt	State = 11111, 100 MHz (RF+ to grounded RF-)	4.19	5.10	6.00	
Parasitic capacitance	Series	All states, 100 MHz (RF+ to GND, RF- to GND)	–	0.5	–	pF
Tuning ratio	Series	100 MHz	–	7.7:1	–	–
	Shunt	100 MHz	–	4.6:1	–	–
Step size	Both	5 bits (32 states), constant step size (100 MHz)	–	0.129	–	pF
Equivalent series resistance	Series	State = 00000	–	1.40	–	Ω
		State = 11111	–	1.33	–	
Quality factor (C_{min}) ⁽¹⁾	Shunt	100 MHz with L_s removed 1 GHz with L_s removed 2 GHz with L_s removed 3 GHz with L_s removed	–	10 35 32 25	–	–
Quality factor (C_{max}) ⁽¹⁾	Shunt	100 MHz with L_s removed 1 GHz with L_s removed 2 GHz with L_s removed 3 GHz with L_s removed	–	27 25 11 6	–	–
Self-resonant frequency (SRF)	Shunt	State = 00000 State = 11111	–	7.5 3.1	–	GHz
Second-order harmonics ($2f_o$) ⁽²⁾	Series	100 MHz–3 GHz	–	–	-36	dBm
Third-order harmonics ($3f_o$) ⁽²⁾	Series	100 MHz–3 GHz	–	–	-36	dBm
Second-order intercept point	Series	100 MHz–3 GHz, +18 dBm per tone, 1-MHz spacing	–	105	–	dBm
Third-order intercept point	Series	100 MHz–3 GHz, +18 dBm per tone, 1-MHz spacing	–	65	–	dBm
Switching time ⁽³⁾⁽⁴⁾	Both	50% CTRL to 10/90% delta capacitance between any two states.	–	–	12	μs
Startup time ⁽³⁾	Both	Time from V_{DD} within the specification to all performances within the specification.	–	–	100	μs

Parameter	Config.	Condition	Min	Typ	Max	Unit
Wake-up time ⁽³⁾⁽⁴⁾	Both	State change from standby mode to RF state to all performances within the specification.	–	–	100	µs

- Notes:
- 1. Q for a shunt DTC is based on a series RLC equivalent circuit. $Q = X_C/R = (X - X_L)/R$, where $X = X_L + X_C$, $X_L = 2 \times \pi \times f \times L$, $X_C = -1/(2 \times \pi \times f \times C)$, which is equal to removing the effect of parasitic inductance L_S .
 - 2. In series or shunt between 50Ω ports. Pulsed RF input with 4620-µs period, 50% duty cycle, measured per 3GPP TS 45.005.
 - 3. To achieve the specified performance, provide a DC path to ground at RF+ and RF-.
 - 4. State change activated on the falling edge of SEN following the data word.

Typical performance data

Figures 2–10 show the typical performance data at +25 °C and 2.6V, unless otherwise specified.



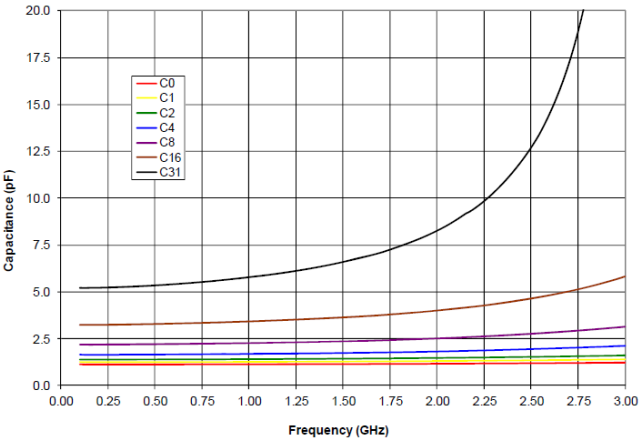


Figure 6. Measured shunt C vs. frequency (major states)

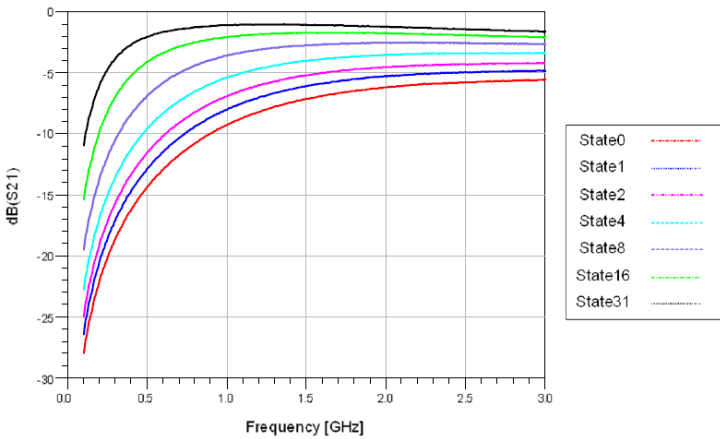


Figure 7. Measured series S_{21} vs. frequency (major states)

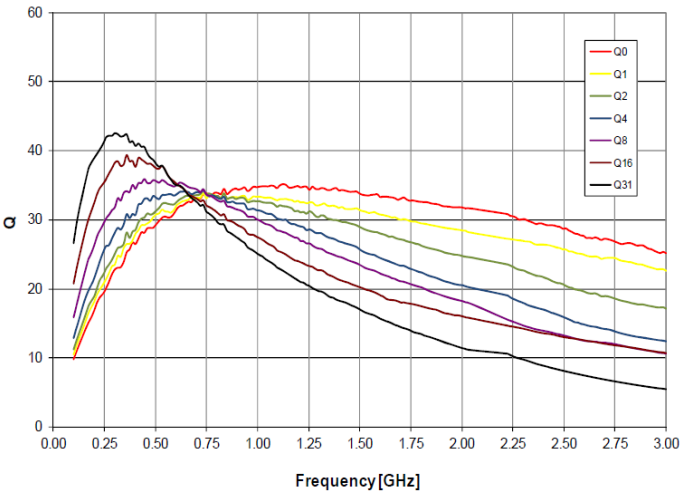


Figure 8. Measured shunt Q vs. frequency (major states)

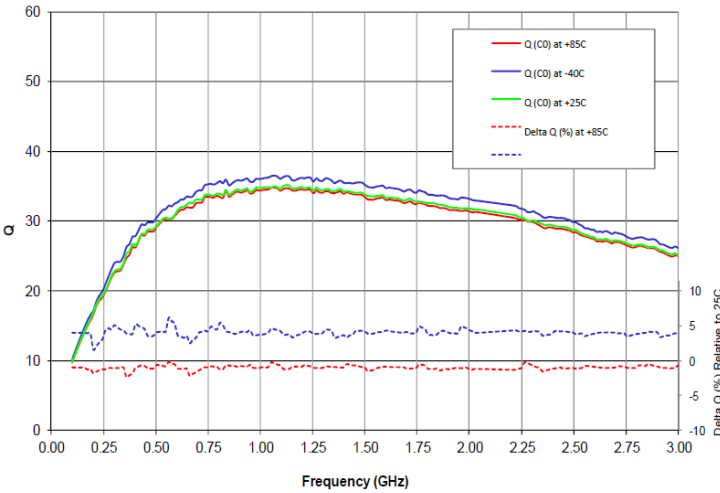


Figure 9. Measured shunt Q (state 0) vs. frequency (temperature)

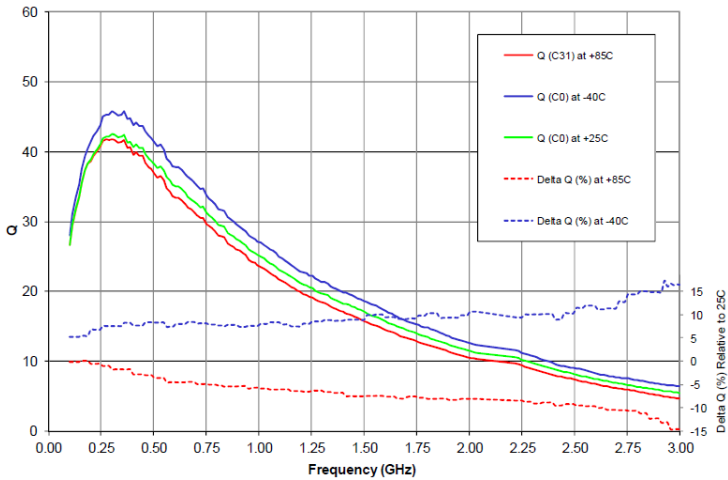


Figure 10. Measured shunt Q (state 31) vs. frequency (temperature)

Operation at frequencies below 100 MHz

You can operate the PE64904 below the 100 MHz specified minimum operating frequency. The total capacitance and peak operating RF voltage are de-rated down to 1 MHz. Figure 11 shows the total shunt capacitance from 1–100 MHz. As seen in Figure 12, the maximum RF voltage that can be placed across the RF terminals or across either RF terminal to ground is de-rated as a function of frequency.

Note: The performance specifications in [Table 3](#) are not guaranteed below 100 MHz. Figures 11, 12, and 13 reflect the performance of a typical PE64904 operated below 100 MHz.

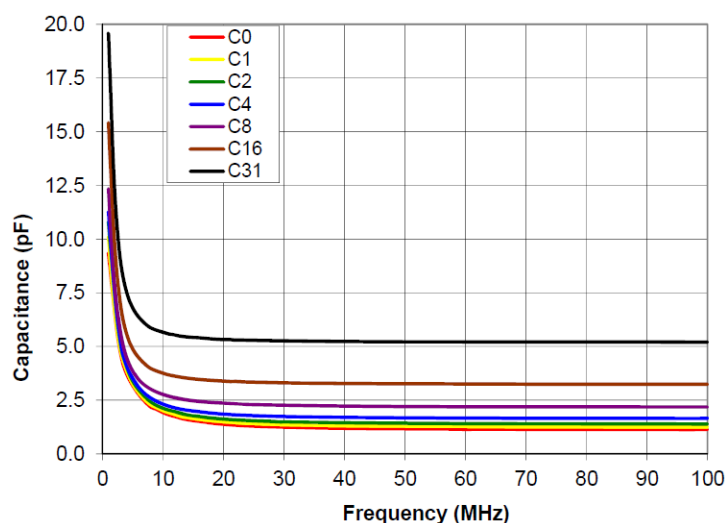


Figure 11. Measured shunt C vs. frequency (major states, 1–100 MHz)

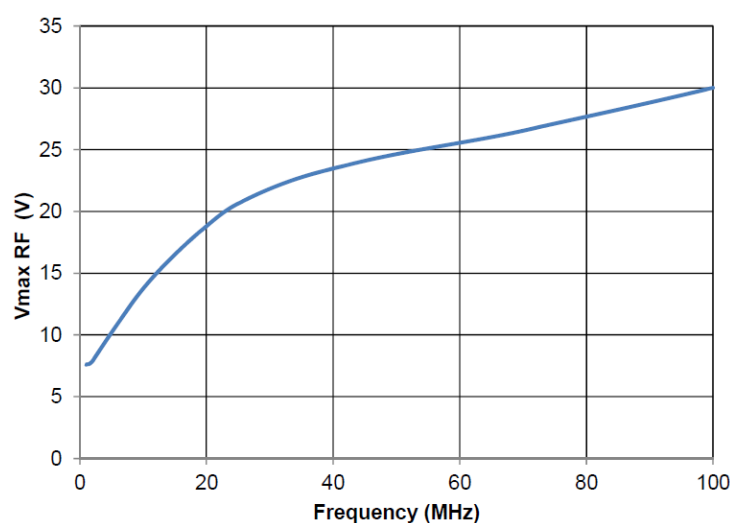


Figure 12. Voltage de-rating vs. frequency (1–100 MHz)

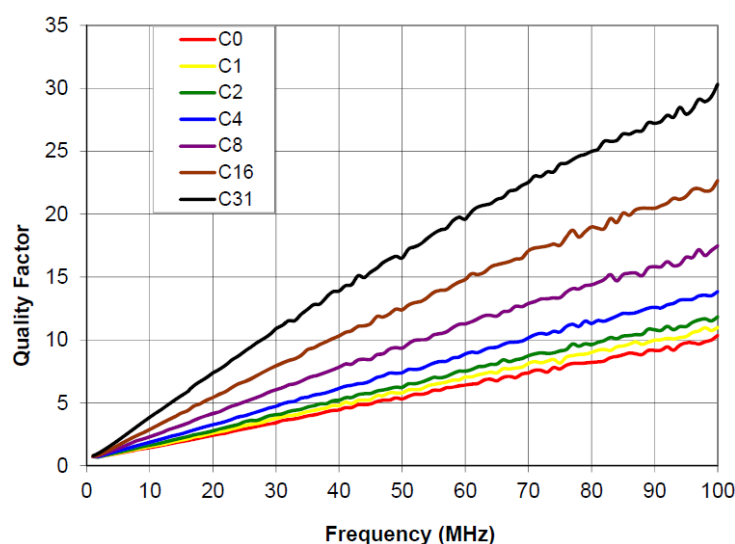


Figure 13. Measured shunt Q vs. frequency (major states, 1–100 MHz)

Serial interface operation and sharing

The PE64904 is controlled by a 3-wire SPI-compatible interface. As shown in Figure 14, the serial master initiates the start of a telegram by driving the Serial Enable (SEN) line high. Each bit of the 8-bit telegram is clocked in on the rising edge of the Serial Clock (SCL) line. The Serial Data (SDA) bits are clocked by the most significant bit (MSB) first, as shown in Table 4 and Figure 14. Transactions on SDA are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last eight bits it received.

You can control multiple DTCs with a single interface by using a dedicated enable (SEN) line for each DTC. The SDA, SCL, and V_{DD} lines can be shared, as shown in Figure 15. The dedicated SEN lines act as a chip select, so each DTC only responds to serial transactions intended for it. This makes each DTC change states sequentially as it is programmed.

Alternatively, you can use a dedicated SDA line with a common SEN. This allows all DTCs to change states simultaneously but requires all DTCs to be programmed even if the state is not changed.

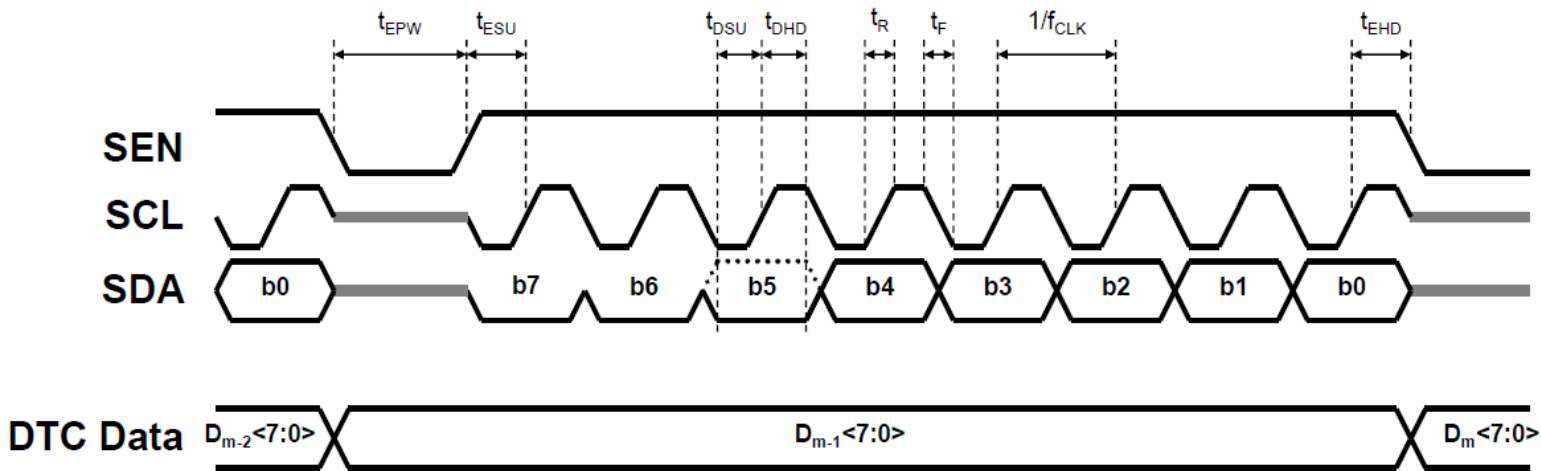


Figure 14. Serial interface timing diagram (oscilloscope view)

Table 4. 6-bit serial programming register map

b7	b6	b5	b4	b3	b2	b1	b0
0	0	STB(*)	d4	d3	d2	d1	d0
↑ MSB (first in)					LSB (last in) ↑		
Note: * The DTC is active when low (set to 0) and in low-current standby mode when high (set to 1).							

In Table 5, $V_{DD} = 2.6V$ and $-40\text{ }^{\circ}C < T_A < +85\text{ }^{\circ}C$, unless otherwise specified.

Table 5. Serial interface AC characteristics

Parameter	Symbol	Min	Max	Unit
Serial clock frequency	f_{CLK}	–	26	MHz
SCL, SDA, SEN rise time	t_R	–	6.5	ns
SCL, SDA, SEN falltime	t_F	–	6.5	
SEN rising edge to SCL rising edge	t_{ESU}	19.2	–	
SCL rising edge to SEN falling edge	t_{EHD}	19.2	–	
SDA valid to SCL rising edge	t_{DSU}	13.2	–	
SDA valid after SCL rising edge	t_{DHD}	13.2	–	
SEN falling edge to SEN rising edge	t_{EOW}	38.4	–	

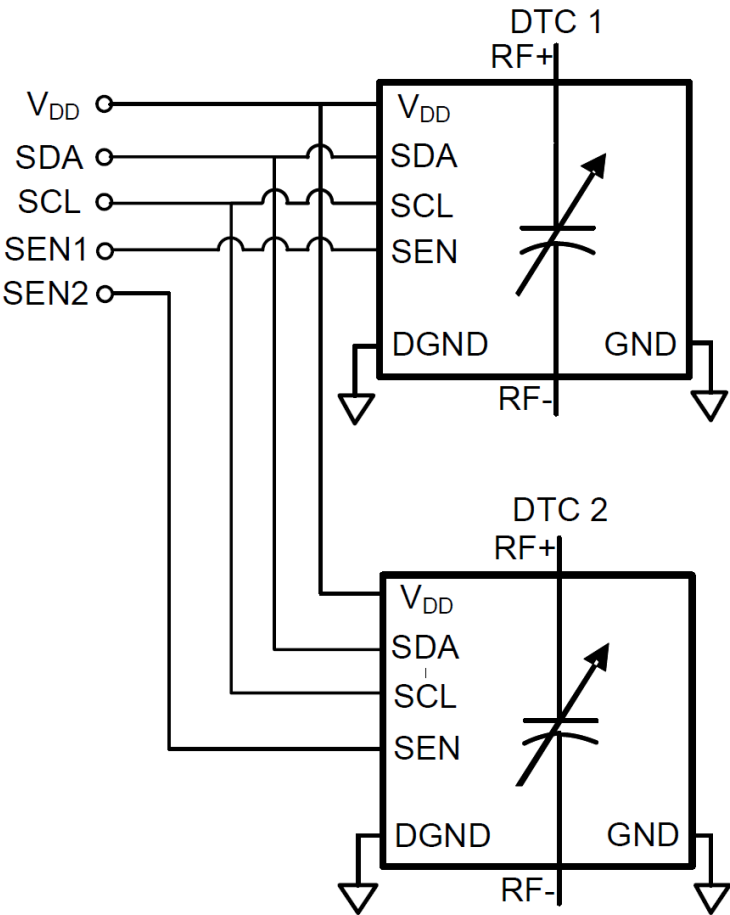


Figure 15. Recommended bus sharing

Equivalent circuit model description

The DTC equivalent circuit model includes all parasitic elements and is accurate in both series and shunt configurations, reflecting physical circuit behavior accurately and providing close correlation to measured data. It can easily be used in circuit simulation programs. Most parameters are state-independent, and simple equations are provided for the state dependent parameters.

The tuning core capacitance C_S represents the capacitance between the RF+ and RF- ports. It is linearly proportional to the state (0 to 31 in decimal) in a discrete fashion. The series tuning ratio is defined as C_{Smax}/C_{Smin} .

C_P represents the circuit and package parasitics from the RF ports to GND:

- In shunt configuration, the total capacitance of the DTC is higher due to the parallel combination of C_P and C_S .
- In series configuration, C_S and C_P do not add in parallel and the DTC appears as an impedance transformation network.

Parasitic inductance due to the circuit and package is modeled as L_S and causes the apparent capacitance of the DTC to increase with frequency until it reaches the self-resonant frequency (SRF). The SRF value depends on the state and is approximately inversely proportional to the square root of the capacitance.

The DTC overall dissipative losses are modeled by the R_S , R_{P1} , and R_{P2} resistors. The R_S parameter represents the equivalent series resistance (ESR) of the tuning core and depends on the state. R_{P1} and R_{P2} represent losses due to the parasitic and biasing networks and are state-independent.

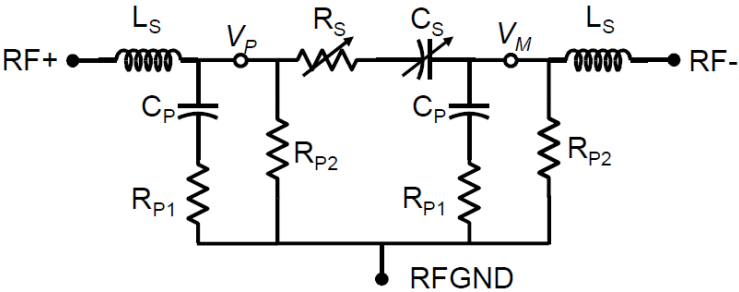


Figure 16. Equivalent circuit model schematic

Table 6. Equivalent circuit model parameters

Variable	Equation (state = 0, 1, 2 ... 31)	Unit
C_S	$0.129 \times \text{state} + 0.600$	pF
R_S	$20 / (\text{state} + 20 / (\text{state} + 0.7)) + 0.7$	Ω
R_{P1}	7	Ω
R_{P2}	10	Ω
C_P	0.5	pF
L_S	0.27	nH

Table 7. Maximum operating RF voltage

Condition	Limit
V_P to V_M	30 V_{PK}
V_P to RFGND	30 V_{PK}
V_M to RFGND	30 V_{PK}

Table 8. Equivalent circuit data

State		DTC core	
Binary	Decimal	C _S (pF)	R _S (Ω)
00000	0	0.60	1.40
00001	1	0.73	2.27
00010	2	0.86	2.83
00011	3	0.99	3.08
00100	4	1.12	3.12
00101	5	1.25	3.05
00110	6	1.37	2.93
00111	7	1.50	2.78
01000	8	1.63	2.64
01001	9	1.76	2.51
01010	10	1.89	2.39
01011	11	2.02	2.27
01100	12	2.15	2.17
01101	13	2.28	2.08
01110	14	2.41	2.00
01111	15	2.54	1.93
10000	16	2.66	1.86
10001	17	2.79	1.80
10010	18	2.92	1.75
10011	19	3.05	1.70
10100	20	3.18	1.65
10101	21	3.31	1.61
10110	22	3.44	1.57
10111	23	3.57	1.54
11000	24	3.70	1.51
11001	25	3.83	1.48
11010	26	3.95	1.45
11011	27	4.08	1.42
11100	28	4.21	1.40
11101	29	4.34	1.37

State		DTC core	
Binary	Decimal	C _S (pF)	R _S (Ω)
11110	30	4.47	1.35
11111	31	4.60	1.33

Layout recommendations

For optimal results, place a ground fill directly under the DTC package on the PCB. Layout isolation is essential between all control and RF lines. When using the DTC in a shunt configuration, verify that the RF- pin is solidly grounded to a filled ground plane. To minimize inductance, verify that the ground traces are as short as possible. A continuous ground plane is preferable on the top layer of the PCB. When multiple DTCs are used together, minimize the physical distance between them. To minimize series parasitic inductance, verify that the connection is as wide as possible.

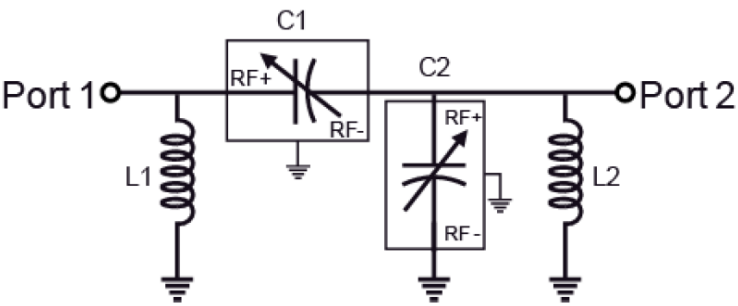


Figure 17. Recommended schematic for multiple DTCs

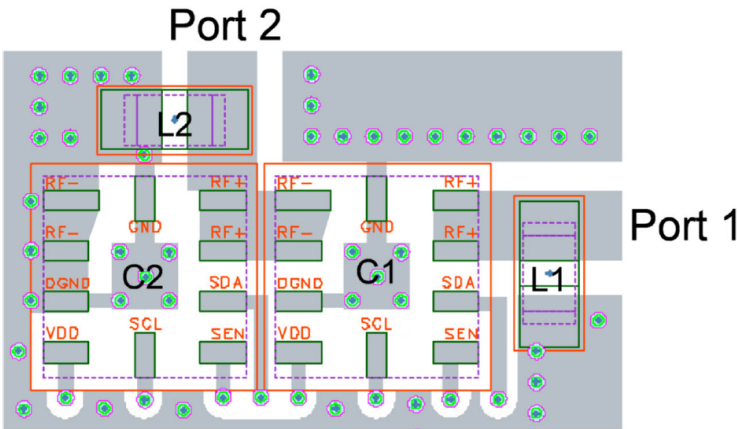


Figure 18. Recommended layout for multiple DTCs

Evaluation board

pSemi designed the 101-0597 evaluation board (EVB) for accurate measurement of the DTC impedance and loss. Two configurations are available:

- 1-port shunt (J3), and
- 2-port series (J4, J5)

Three calibration standards are provided. The open (J2) and short (J1) standards (104-ps delay) are used to perform port extensions and account for electrical length and transmission line loss. Use the Thru (J9, J10) standard to estimate the PCB transmission line losses for scalar de-embedding of the 2-port series configuration (J4, J5).

The board consists of a 4-layer stack with two outer layers made of Rogers 4350B ($\epsilon_r = 3.48$) and two inner layers of FR4 ($\epsilon_r = 4.80$). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

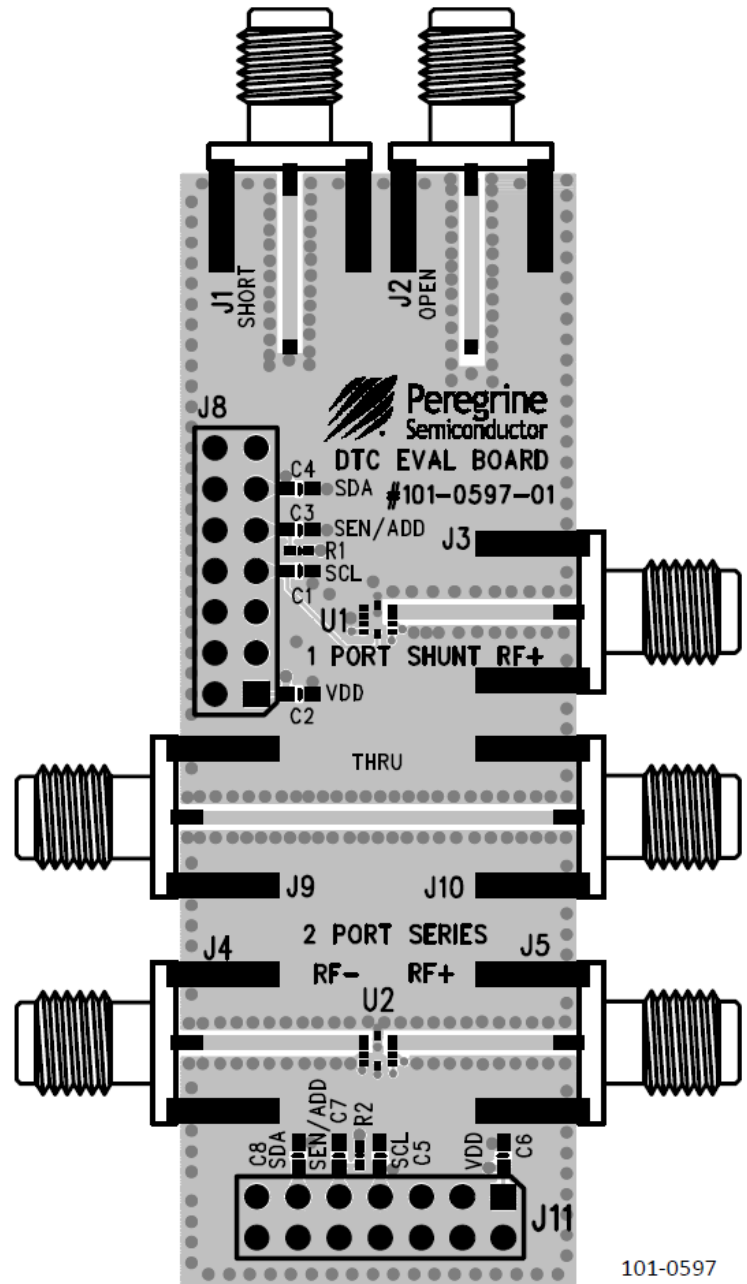


Figure 19. Evaluation board layout

Pin configuration

Figure 20 shows the PE64904 pin configuration for the 10-lead $2 \times 2 \times 0.45$ mm QFN package, and Table 9 lists the description for each pin.

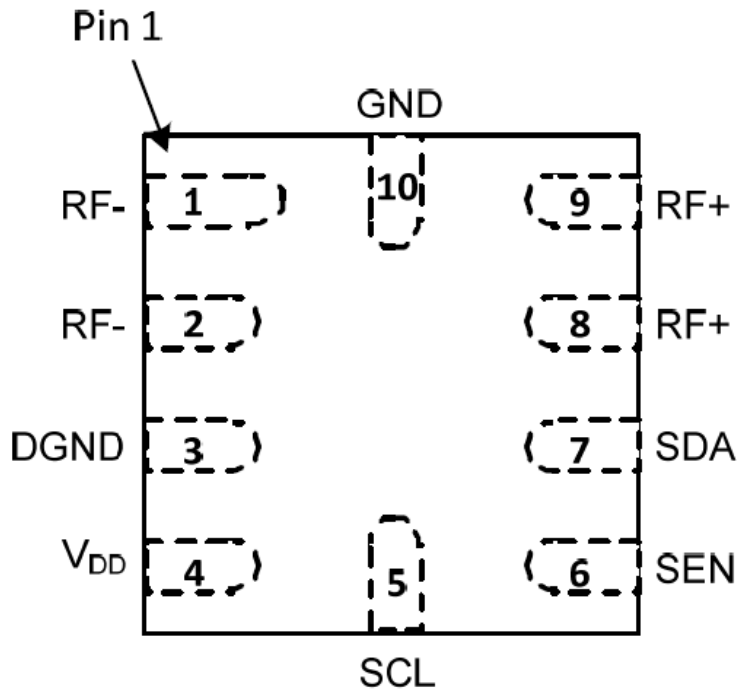


Figure 20. Pin configuration, top view

Table 9. Pin descriptions

Pin no.	Pin name	Description
1, 2 ⁽¹⁾	RF-	Negative RF ports
3	DGND	Ground
4	V _{DD}	Supply voltage
5	SCL	Serial interface clock input
6	SEN	Serial interface latch enable input
7	SDA	Serial interface data input
8, 9 ⁽²⁾	RF+	Positive RF ports
10	GND	RF ground

Notes:

- For optimal performance, tie RF- pins 1 and 2 together on the PCB.
- For optimal performance, tie RF+ pins 8 and 9 together on the PCB.

Packaging information

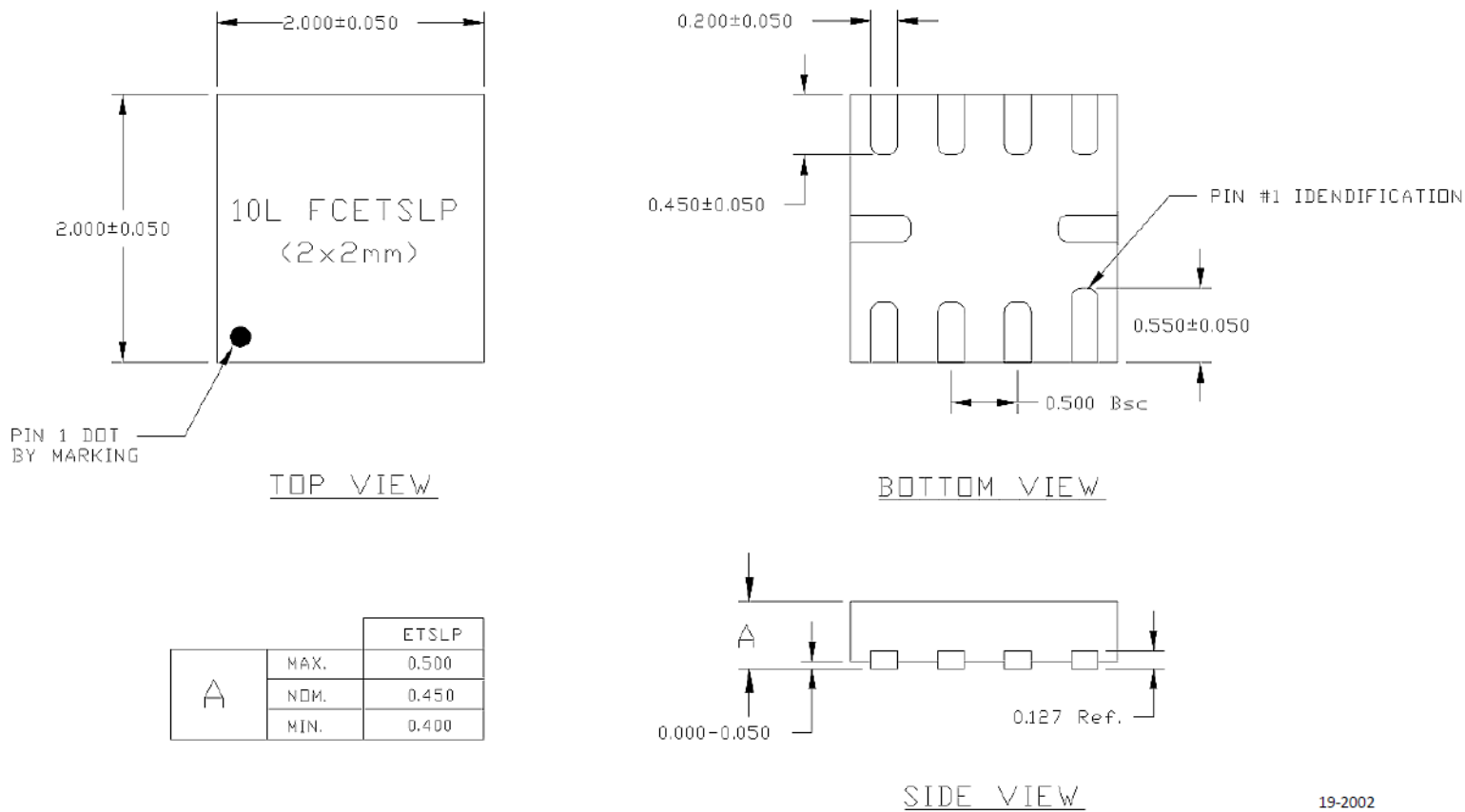
This section provides the following packaging data:

- Moisture sensitivity level
- Package marking
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE64904 moisture sensitivity level rating for the 10-lead 2 × 2 × 0.45 mm QFN package is MSL3.

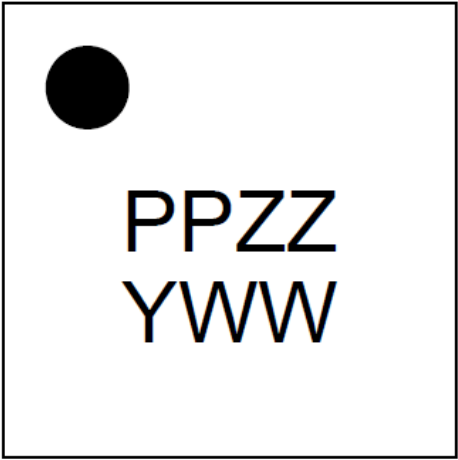
Package drawing



19-2002

Figure 21. Package mechanical drawing for the 10-lead 2 × 2 × 0.45 mm QFN package

Top-marking specification



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	CG	Part number marking for PE64904
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Figure 22. PE64904 package marking specification

Tape and reel specification

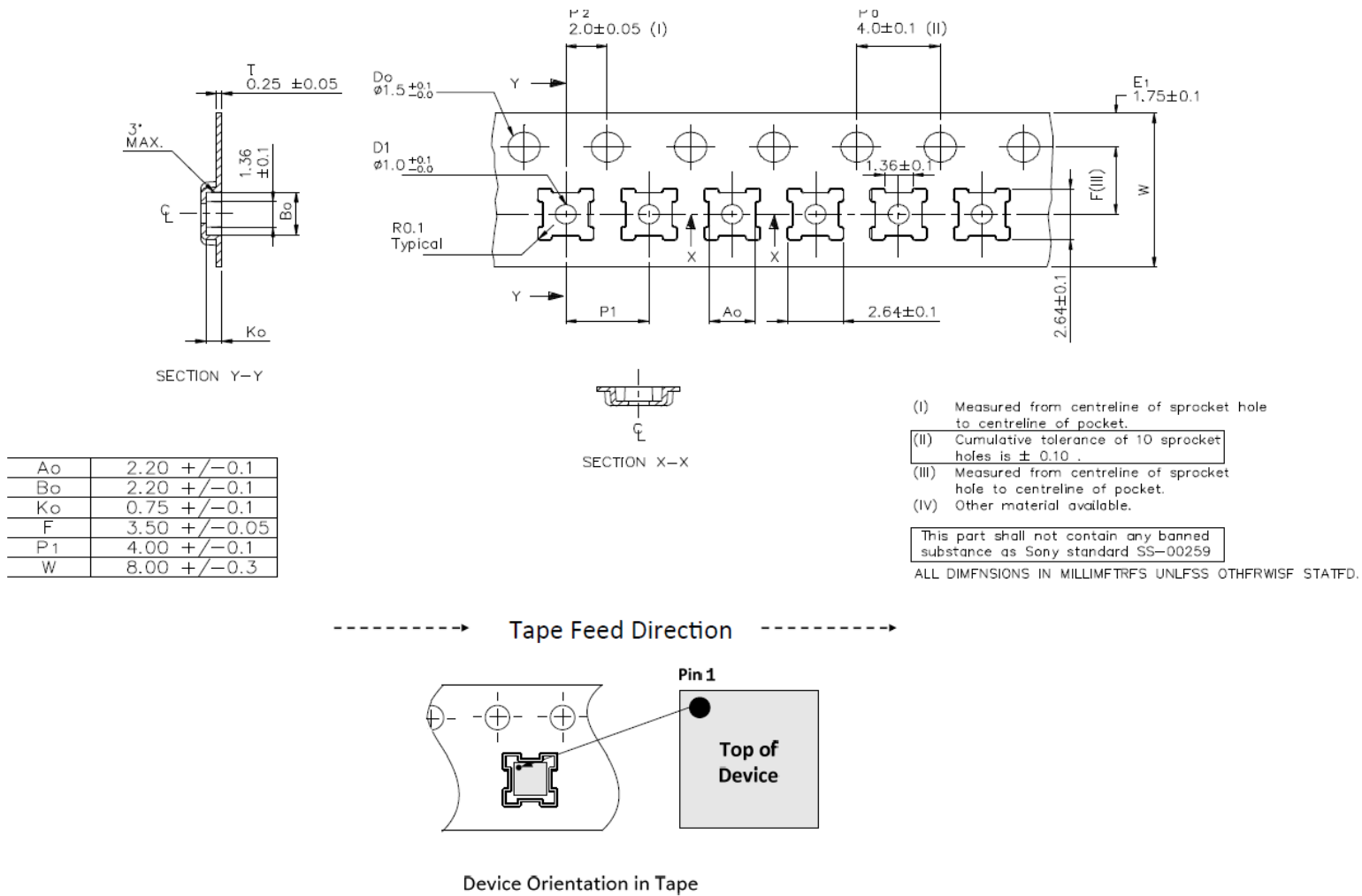


Figure 23. Tape and reel specification for the 10-lead 2 × 2 × 0.45 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE64904D-Z	PE64904 UltraCMOS® digitally tunable capacitor	10-lead 2 × 2 × 0.45 mm QFN	3000 units/T&R
EK64904-14	PE64904 evaluation kit	Evaluation kit	1/box

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